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Contract No. NAS8-32607
Supplemental Agreement No. 2

DESIGN, PROCESSING AND TESTING OF LSI ARRAYS
HYBRID MICROELECTRONICS TASK

28 SEPTEMBER 1978 - 28 SEPTEMBER 1979

15 OCTOBER 1979

Prepared for
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HYBRID MICROELECTRONICS TASK

1.0 INTRODUCTION AND SUMMARY

This report summarizes a twelve-month effort on Contract NAS 8-32607, Supplementary Agreement No. 2; and completes the second year of such effort, starting with the 1977-1978 cost-factors/packaging program. Specifically, this program involves determination of those factors affecting the cost of electronic subsystems utilizing LSI microcircuits, and development of the most efficient methods for low-cost packaging of LSI devices as a function of density and reliability. Overall program Tasks are summarized in Figure 1-1.

This one-year supplementary program has been divided into two Tasks as follows:

TASK A - Cost Factors Study

Mathematical cost factors were generated under the original contract for both hybrid microcircuit and printed wiring board (PWB) packaging methods, and a mathematical cost model was created for analysis of microcircuit fabrication costs. Under the Supplementary Agreement effort, the cost model is to be refined and broadened to cover discrete (PWB) packaging techniques, and to include component parts such as ceramic chip carriers, multichip LSI "subassembly" arrays, and plastic LSI packages (all of which may incorporate tape chip carrier interconnection technology). The costing factors previously developed are to be refined and reduced to formulae for computerization.

TASK B - Tape Chip Carrier Development Study

Tape chip carrier technology has been shown under the original contract to represent a viable approach to low cost LSI packaging, with additional potential for lowering the cost of hybrid microcircuit fabrication. Certain technical problem areas, inherent to LSI applications, have been identified; work is to continue during the Supplementary Agreement time period in an effort to resolve these problems by continued development in the areas of wafer bumping, inner/outer lead bonding, testing on tape, and tape processing.

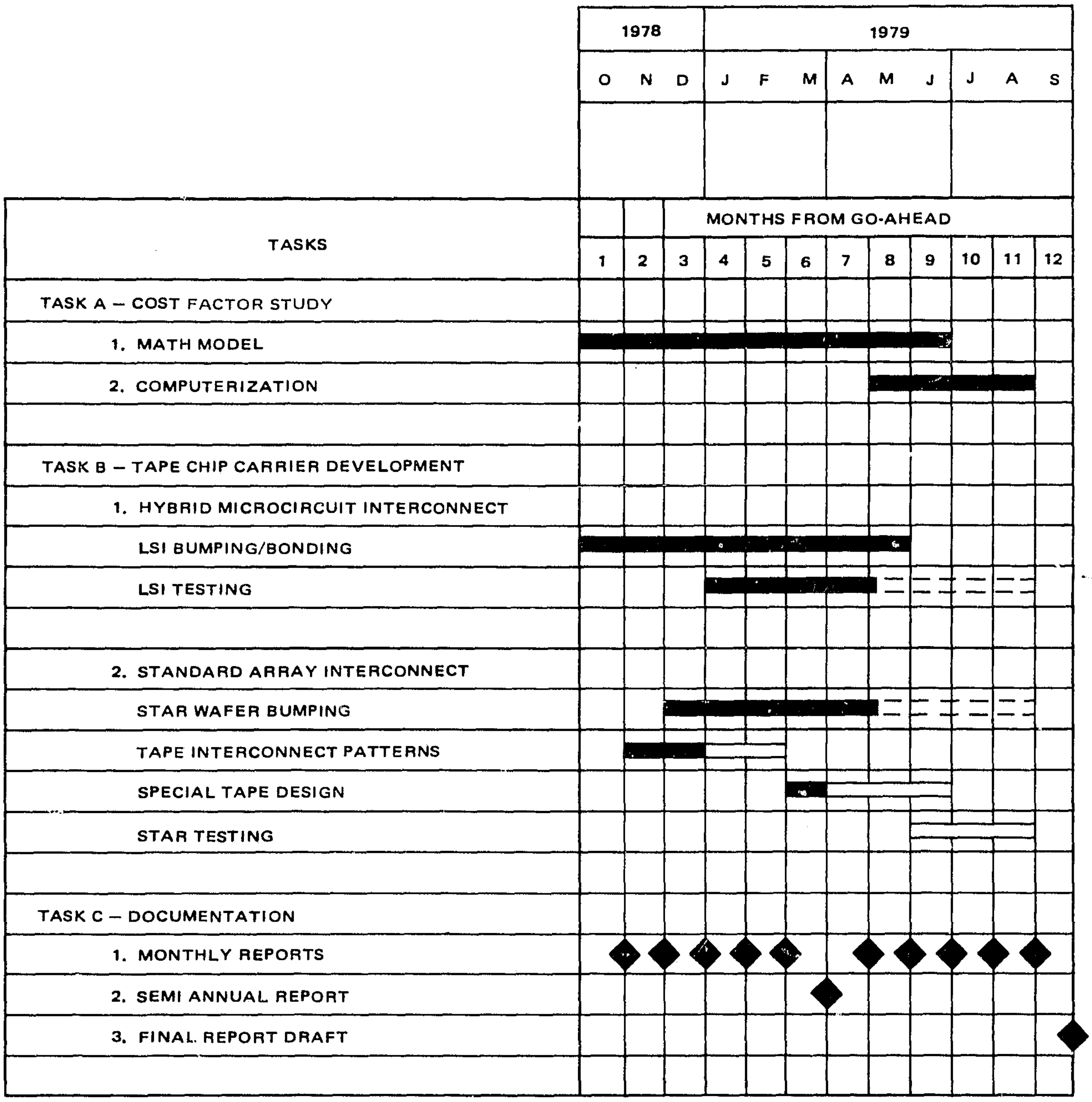

Figure 1-1. Overall program schedule.

Tape chip carrier technology shall be developed further by studies and laboratory effort toward demonstrating the feasibility of interconnecting arrays of two, four, or more LSI chips on the tape carrier. Such arrays would form standard modules or "blocks", from which larger assemblies could be constructed.

TASK A Synopsis

Mathematical cost models previously developed for hybrid microelectronic subsystems have been refined and expanded under Supplementary Agreement No. 2 to include rework terms related to substrate fabrication, non-recurring developmental and manufacturing operations, and prototype production. In addition, sample computer programs have been written to demonstrate hybrid microelectronics applications of these cost models.

Computer programs were generated to calculate and analyze, through the equations of the models developed, values for the total hybrid microelectronics costs. These programs were employed also to calculate cost variations when nonconventional technologies such as the tape chip carrier (which is one method of packaging large scale integrated (LSI) semiconductor devices) become a more widely used part of hybrid microelectronics. In addition, cost surfaces were generated; behavior of the hybrid cost function relative to the total number of chips utilized, and in accordance with expected production volume, was studied over a large range.

Modeling procedures and techniques similar to those developed for hybrid microelectronics applications were employed to model conventional printed wiring board packaging processes. The total manufacturing cost of a fully assembled printed wiring board (PWB) structure, including electronic component parts, was expressed in terms of PWB fabrication, assembly to PWB substrates, and nonrecurring/recurring materials costs. The qualitative cost factors collected from previous work[*(1)] were quantified by analyzing worksheets from several PWB facilities. These costs have been correlated to their respective process parameters for each step of the process.

The models developed during the first-year effort[(1)] were valid only when applied to volume runs on the order of 120,000 units yearly.

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*(References are listed in Appendix "A".)

Improvements of these mathematical cost models during this second-year period include the following areas:

1. Substrate Fabrication
   a. Rework cycles and inspection steps have been added.
   b. Yield of the fabrication process has been expressed in terms of rework.
2. Total Hybrid Microelectronics Subsystem Fabrication
   a. Non-recurring developmental and manufacturing costs have been included in the equations.
   b. Production volume has been introduced as a variable parameter in the equation.
   c. Values of constants, and those parameters defining the reference hybrid, have been reestablished to include the impact of prototype production.

To compute and analyze relationships between the cost of each process step and the process parameters involved, computer programs have been written. One of these programs generates a three-dimensional cost surface, which permits visual interpretation of the cost-process parameters relationship. A graphical display such as this is better understood and more readily related to personal experience than is any other display form.

The mathematical models developed for both hybrid microelectronics and printed wiring board technology eventually can be refined such that the computer can be used for developing cost estimates (in job bidding) within a 15-percent accuracy for well-defined cases. Accuracy was not the primary concern of this program however; rather, the major concern was to develop models which were capable of handling a large variety of electronics technologies, and to obtain comparative costs of the various technological approaches. By recognizing program goals, and by clearly stating the boundary conditions which must be satisfied each time a given electronics subsystem is considered, the models developed could be successful tools to analyze the cost of any electronic subsystem, and to evaluate associated technologies.

The purpose of this work is to develop a tool to evaluate the entire hybrid microelectronics fabrication cost when technological changes are made in any portion of the processes involved. In this way, those changes which are associated with cost reductions will become more readily identifiable; currently, they are hidden in the literature, or in the practical knowledge of a few qualified people.

The ability to predict cost consequences when a change in technology is made is a major factor in bringing about reduced production costs. Coincidentally, in seeking cost savings, new technological approaches are derived. The models therefore will have served their purpose if, besides identifying those areas which will impact cost savings directly, they also help to identify those additional technological improvements necessary to cause further savings.

TASK B Synopsis

Task B has two basic parts. In the first part, developmental work has continued on LSI packaging utilizing tape chip carrier (TCC) technology, particularly in the areas of tape processing, wafer bumping, and inner/outer lead bonding. In the second part, studies and laboratory efforts have been utilized to show the feasibility of interconnecting arrays of LSI chips utilizing tape chip carrier and semiautomatic wire bonding technology.

Table 1-1 is a work approach matrix which outlines those tape chip carrier tasks completed under the original contract, and which indicates the direction of effort which has been undertaken during the Supplementary Agreement time period on a Task/Goal basis. Specific semiconductor device types are listed and identified by code letter.

Subtask Numbers 8 (Lead Finger Support) and 12 (Silicon Nitride Coating/Retest) were included for target or "best efforts" investigations as time and funding considerations permit. The "Lead Finger Support" task covers several techniques/materials which Hughes has been investigating on internal funding during the program time period. This concept involves potential tape carrier yield improvements brought about by inclusion of a soluble organic etched-lead support within the window area.

TABLE 1-1. TAPE CHIP CARRIER WORK APPROACH - TASK B

Task Description	Planned Device Complement	Program Goals	Planning/Execution			
			25	50	75	100
1. Wafer Bumping	B, C, D, E, G	More Definitive Process Refinement Required				
2. Wafer Characterization (Before/After Bumping)	D, E	To be Conducted Jointly with Suppliers				
3. Tape Preparation	D, E, and G (A, B, C as required)	Expansion to 6-in. and/or 12-in. Lengths				
4. ILB	D, E, and G (complete C)	Use of Projected New IMI Production Bonder				
5. Testing on Tape	D, E, and G (complete C)	Functional Testing				
6. Burn in on Tape	A (possibly D and E)	Demonstration				
7. Excise/Forming	D, E, and G (complete C; Excise only for HCCs)	C: Use Newly-Received Tool; Procure New Tool				
8. Lead Finger Support	B, C, D, E, and G (best efforts)	Investigate for ILB Compatibility, Solubility				
9. OLB to S/F Newworks	A and G	Multilayer Circuitry				
10. OLB to HCCs	Complete B and C; possibly D and E	Process Demonstration, Refinement				
11. Reliability Testing of Networks/HCCs	E (possibly B and G)	Pressure Cooker Test, Thermal Cycling, HTRB; Both HCCs and Networks				
12. Silicon Nitride	Best Efforts: A, B, C, D, E, and G	Potential Replacement for Hermetic Packages				
13. Multiple-Chip TCC or Wire-Bond	Best Efforts: E	Initial Conceptual Investigation and Proof-of-Performance				

Planned Devices:

A: 14-Pad Type 5400/54LS00 Dual Quad NAND Gates (Fchld.)

B: 18-Pad Type 1824D Microprocessor RAM (HAC)

C: 82-Pad ECL/MUX, ECL/REG, and/or ECL/MAA (Sig.)

D: 40-Pad Type 6402 CMOS UART (Harris)

E: 38-Pad 384-Element STAR (MSFC)

F: 64-Pad 1584-Element STAR (MSFC)

G: 35-Pad Type 342 CMOS Digital Correlator (HAC)

The Silicon Nitride Coating/Retest effort refers to a current U.S. Air Force (AFML) Manufacturing Technology Program with Hughes-Culver City (Contract F33615-77-C-5049), in connection with which Hughes-Newport Beach currently is conducting reliability investigations. A production reactor offering relatively-low-temperature (150°C) Si_3N_4 coating of hybrid microcircuits, tape-carrier-mounted devices, and/or packaged semiconductors was installed at the Newport Beach facility during July, 1979. Implementation delays have prevented investigations during this program time period concerning effectivity of Si_3N_4 coating over tape-mounted devices. Such efforts will be proposed for future investigations.

Under Subtask 13, studies and developmental effort were to have been applied to interconnection of standard array LSI devices, in groups of two, four, or more, in an effort to bring about a cost effective and versatile packaging method for minicomputers and high density memory arrays. This Subtask has not been accomplished during the Supplementary Agreement No. 2 time period because of delays in procurement of those standard array devices planned as test vehicles for this developmental effort; namely, the NASA-developed STAR (Standard Transistor Array Radix). The STAR design system is a double-metal semi-custom approach to generating quick-turnaround MOS digital LSI circuits. It consists of an array of devices defined in different technologies with a common grid system. The arrays are processed to the point of metal definition and held in storage. STAR circuit interconnection designs are created by three custom masks that define the first level of metal, the via mask, and the second level of metal. The STAR has been defined by NASA in the CMOS-BULK metal gate, CMOS-SOS silicon gate, CMOS-BULK silicon gate, CCL-SOS, and CCL-BULK technologies. A family of 22 logic cells have been designed and digitized by NASA for use with STAR arrays, which are being created in different sizes, ranging from an equivalent 384 transistors up to an equivalent 5264 transistors.

STAR technology offers many advantages of custom integration such as reliability, secrecy, power, and size reduction, while allowing faster turn-around time and lower cost than that possible with custom integration

techniques. In Subtask 13, the objectives of low cost and fast turn-around will be extended to the next level: packaging of STAR devices. Although such packaging could not be accomplished during the time period of this Supplementary Agreement No. 2, it will be proposed as a portion of a potential follow-on Supplementary-Agreement-No. -3 effort.

Section 2. 0 includes a more detailed description of Task A and B progress during this program.

DESIGN, PROCESSING AND TESTING OF LSI ARRAYS
HYBRID MICROELECTRONICS TASK

2.0 TECHNICAL DISCUSSION

Mathematical model refinement under Task A has been completed, as indicated in Section 1.0, and summarized in the Cost Factors Program Schedule of Figure 2-1. Considerable Tape Chip Carrier (TCC) process refinement progress has been made under Task B; bump processing of the 1.5-inch-diameter x 0.008-inch mechanical sample STAR wafers received from MSFC has been initiated, but assembly of bumped arrays was not completed during the Supplementary Agreement No. 2 time period. This task will be included as part of a potential follow-on program to be proposed as Supplementary Agreement No. 3.

2.1 TASK A – COST FACTORS

Substrate fabrication flow charts for thin and thick film technology were modified during the first six months of this program time period to include inspection/quality-control steps and rework cycles. The addition of rework cycles in the models permits process yield expression on an explicit basis, thus eliminating the previously defined need for expressing an additional yield parameter independent of process parameters.

Equations representing substrate (ceramic-based network) fabrication consequently have been modified by the addition of two new parameters: (a) Inspection cost, and (b) Number of rework cycles; in addition to introduction of new coefficients.

The previously-developed mathematical models were applicable to large production quantities (about 120,000 per year). It consequently was necessary to modify these models so that the total cost of a hybrid microcircuit could be predicted when small production quantities are considered (one to 1500 per year, in lot sizes of one to 100).

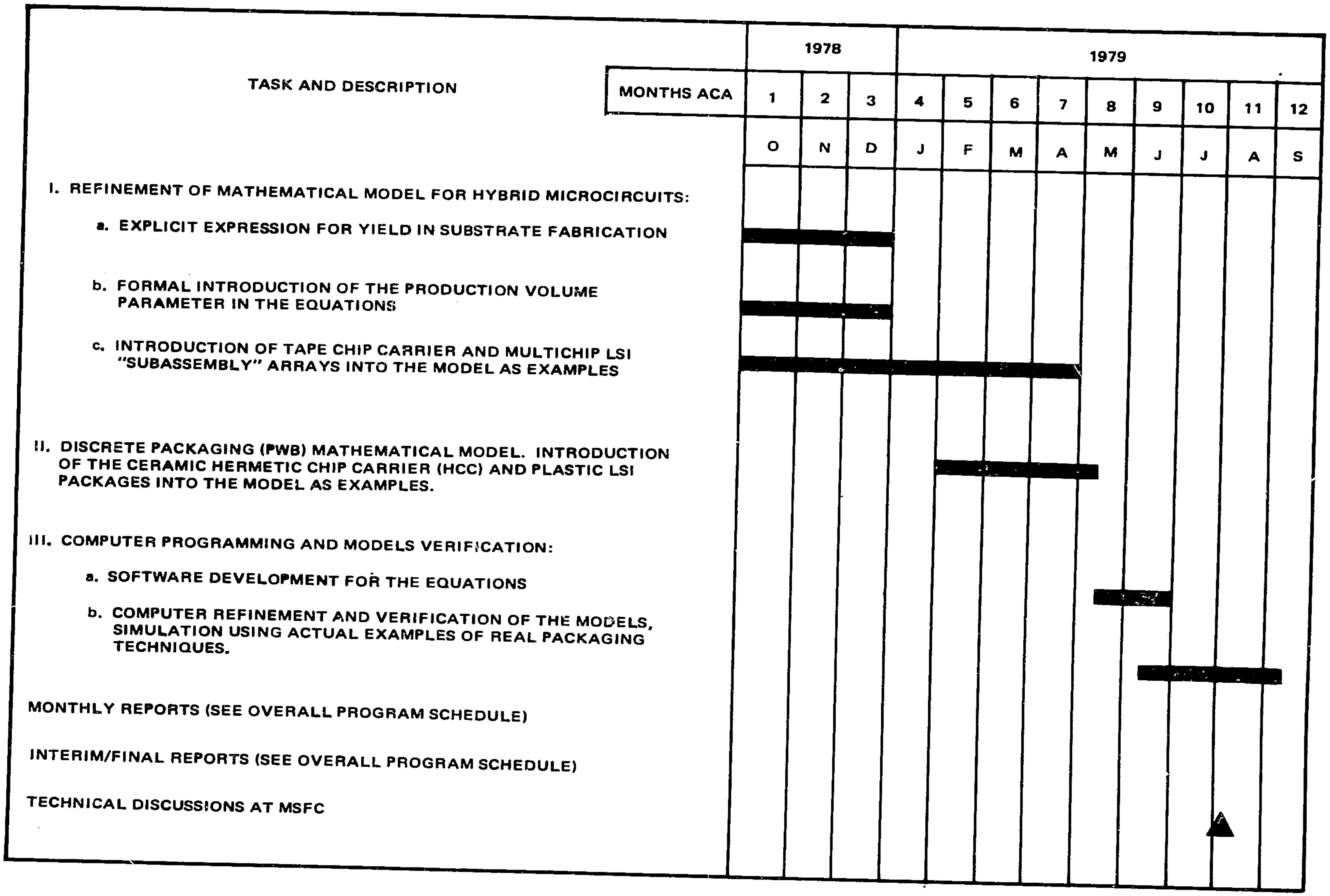


Figure 2-1. Cost factors (task A) program schedule.

The generalization to include small production quantities was made by means of the following two steps: a) Additional cost factors were gathered concerning the production of hybrids in prototype facilities and, b) These costs were introduced as additional terms (and/or multiplying factors) in previously-developed equations.

As a consequence of this generalization, it was found that differentiation of engineering costs between a hybrid build in a prototype facility, and the same hybrid build in a large production facility, was an important consideration. Differences between these hybrids have been expressed quantitatively in graphical form by using a family of curves; and in symbolic form by means of distinct equations. The equations were obtained with the data available by finding the best curve fit using a statistical analysis approach.

In addition to the above-described factors, distinction has been made between recurring and non-recurring costs. These costs now are expressed in the equations as percentages of total manufacturing costs. In this way, the non-recurring engineering costs proportionally change with the total manufacturing cost, and they are affected directly by the degree of hybrid complexity.

Three major categories have been considered for the non-recurring developmental costs: a) Engineering costs, which include items such as applications engineering, design layout, package drawings, and test fixtures design; b) Engineering Proof of Design (POD) models, which include planning for the continuation of production, engineering support, and total fabrication/assembly; and c) Engineering Pre-Production Models, which take into account the costs necessary to build exactly the same hybrids that will be required in production.

Items such as test fixtures, layouts, masks, manufacturing drawings, screens, and instructive photos have been introduced into equations as part of the non-recurring manufacturing costs.

2.1.1 Computer Programming and Model Verification for Hybrid Microelectronics Applications

Equations expressing the total cost of hybrid microelectronics subsystems have been developed*[(1)] and subsequently refined[(2)]. It was found that through simple computer programming, these formulas could furnish comprehensive information about cost functions otherwise not readily evident. In turn, this information was used to refine functional relationships between process parameters and those costs developed during the modeling phase of the program. In this way, accuracy of the model and its capability to predict cost trends, both have been improved.

Two computer programs were written; one to compute a single-valued cost function; the other, to generate a cost surface. The single-valued cost function program includes, as a special case, computation of the cost differential when tape chip carrier (TCC) technology is used. The cost factors involved, and the equation developed when this type of technology is applied, previously have been modeled[(1)] according to the simplified process flow shown in Figure 2-2.

For a given set of input variables, the single-valued cost function program computes and prints out complexity factor, substrate fabrication cost, assembly cost, recurring material cost, and total hybrid cost; in addition to cost differential when TCC technology is used.

The entire program to compute a single-valued cost function is reported in Appendix B, and typical print-outs are shown in Figure 2-3. Symbol meanings and the process steps have been included as part of the print-out for easy reading of the equations.

The cost surface program shown in Appendix C generates a matrix of cost values, which then are plotted through any graphical display program to obtain cost surfaces for each couple of desired variables in three dimensions (the third dimension being the cost of the hybrid). Figure 2-4 shows a typical graphical output obtained with this program by selecting the total number of chips and the production rate as variables. Another view of the

*References are listed in Appendix "A".

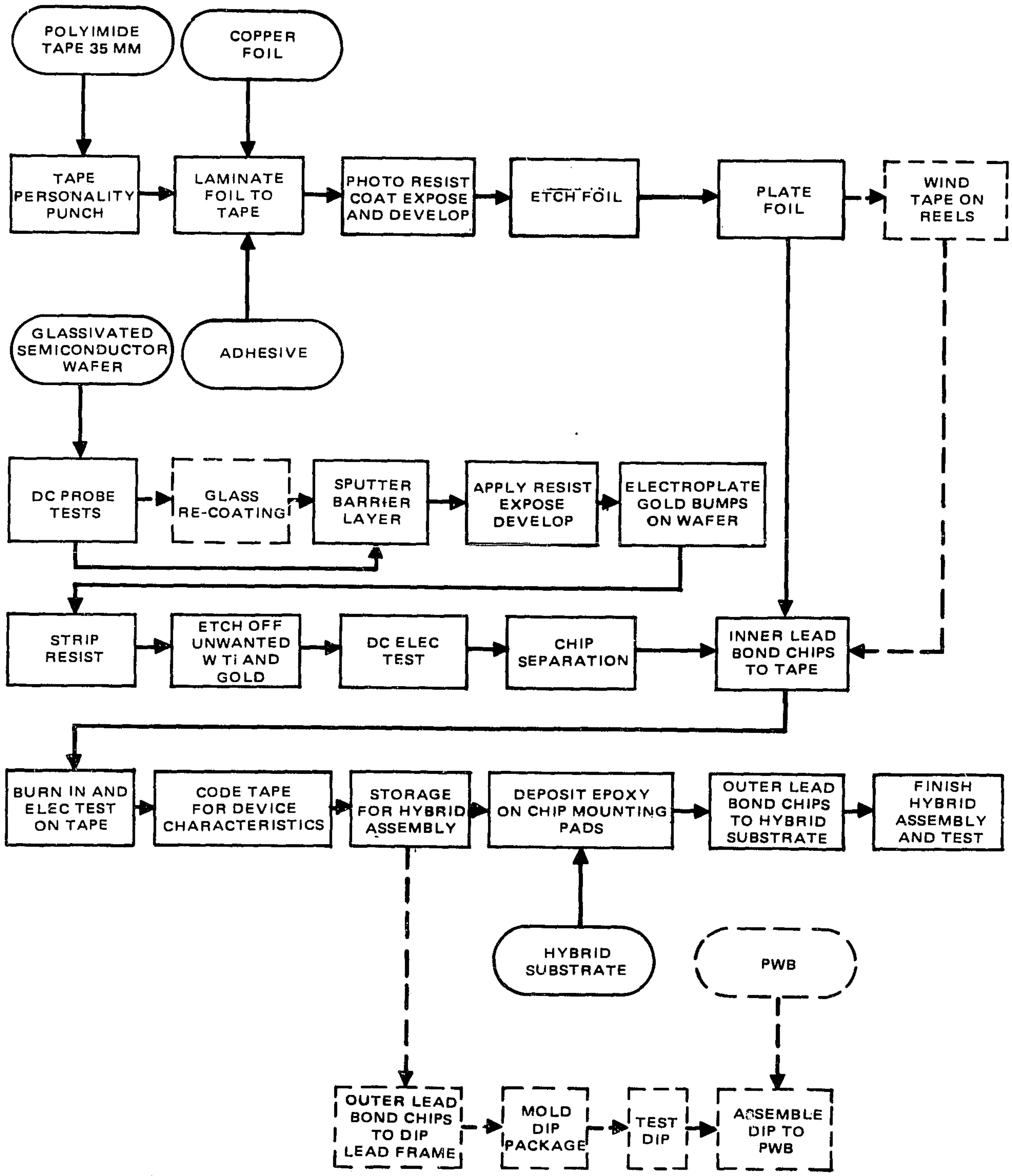


Figure 2-2. Tape chip carrier process flow.

HYBRID MICROELECTRONICS MANUFACTURE: $\upsilon = 10$

COMPLEXITY FACTOR(CC)= 0.44
SUBSTRATE FABRICATION COST(C'SP)= $183.74
ASSEMBLY COST(C'AT)= $1913.66
RECURRING MATERIAL COST(CM)= $117.22
TOTAL HYBRID COST = $2214.62

$\upsilon = 50$

COMPLEXITY FACTOR(CC)= 0.44
SUBSTRATE FABRICATION COST(C'SP)= $96.52
ASSEMBLY COST(C'AT)= $1005.26
RECURRING MATERIAL COST(CM)= $117.22
TOTAL HYBRID COST = $1219.00

$\upsilon = 120{,}000$

COMPLEXITY FACTOR(CC)= 0.44
SUBSTRATE FABRICATION COST(C'SP)= $11.10
ASSEMBLY COST(C'AT)= $115.58
RECURRING MATERIAL COST(CM)= $117.22
TOTAL HYBRID COST = $243.90

HYBRID MICROELECTRONICS MANUFACTURE: $\upsilon = 10$

COMPLEXITY FACTOR(CC)= 0.44
SUBSTRATE FABRICATION COST(C'SP)= $183.74
ASSEMBLY COST(C'AT)= $1913.66
RECURRING MATERIAL COST(CM)= $117.22
TOTAL HYBRID COST = $2214.62

ALTERNATE CASE SELECTED:

EFFECT OF TAPE CHIP CARRIER (TCC) TECHNOLOGY
ON HYBRID MANUFACTURING COST:

TAPE CHIP CARRIER COST DIFFERENTIAL(CTCC)= $421.63
TOTAL HYBRID COST WITH TAPE CHIP CARRIER = $1675.77

Figure 2-3. Single-valued cost function print-out for different production volumes (υ), and for TCC case.

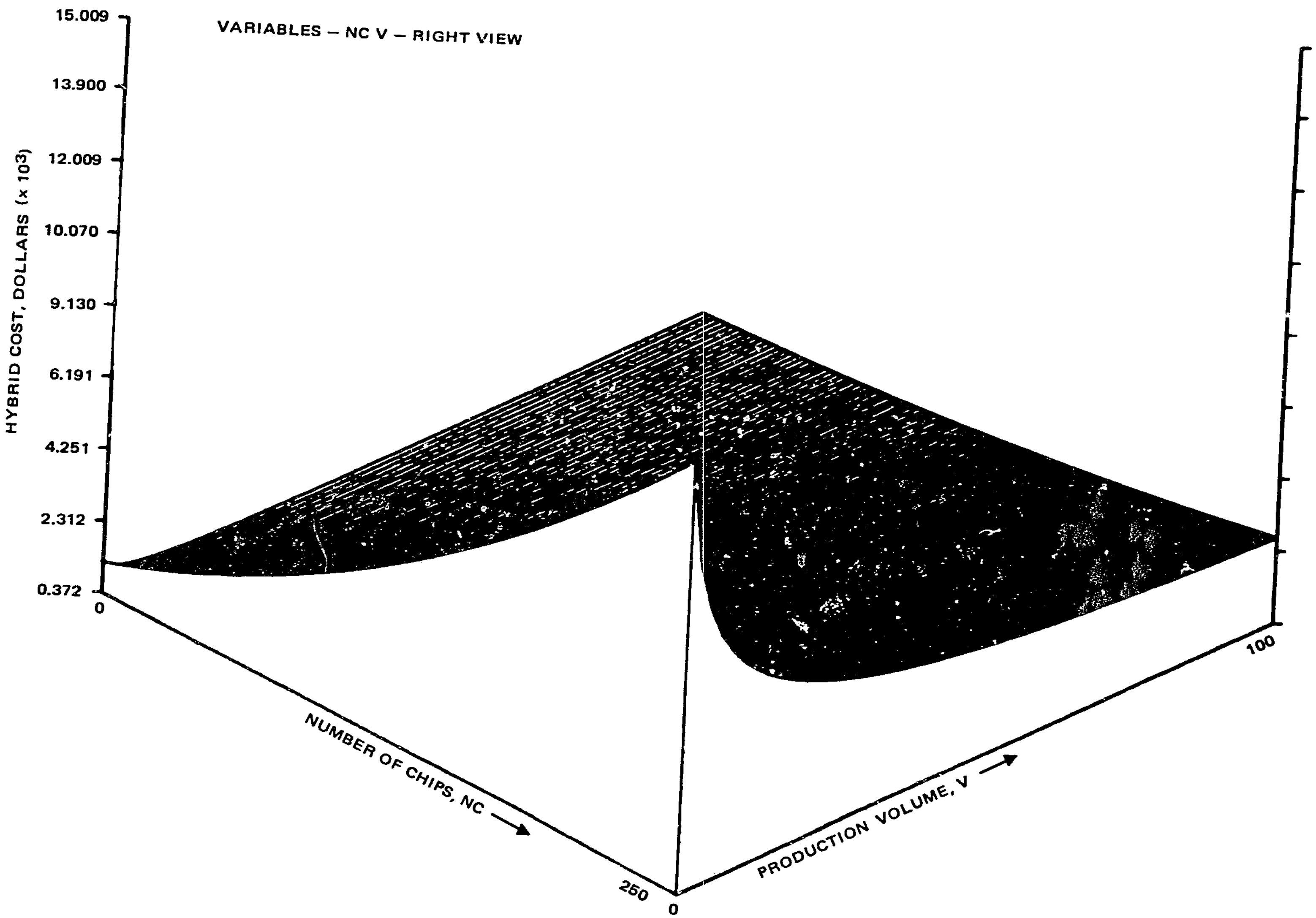


Figure 2-4. Total hybrid cost is a function of total number of drips and production volume (right view).

same variables, obtained by axis rotation, is shown in Figure 2-5. As production volume decreases and the total number of chips increases, the total hybrid cost increases. The exponential behavior of the plot largely is attributable to the non-linear dependence of the cost function with respect to production volume.

2.1.2 Modeling to Develop Total Manufacturing Cost of Conventional Packaging via Printed Wiring Board (PWB) Technology

The cost in dollars of a PWB electronics module (CPWB) which includes assembled electronics component parts, is modeled by the following equation:

$$CPWB = CPMFAB + CPRMA + CMRF + CMRA, \qquad (1)$$

where CPMFAB is PWB fabrication cost, CPRMA is cost of the assembly of electronic component parts on the PWB, CMRF is recurring material fabrication cost, and CMRA is recurring material assembly cost.

Production volume and non-recurring costs are not explicitly expressed in Equation (1), but contained in the CPMFAB and CPRMA terms. Functionally however, CPWB is related to production volume (V), and to non-recurring costs by a relationship of the type:

$$CPWB = CWB\ P(P_1, P_2, CCF)\ F(V); \qquad (2)$$

where CWB is the non-recurring and volume-independent total PWB manufacture cost, and $P(P_1, P_2 = CCF)$ is defined by a relationship of the type:

$$P + (P_1 + P_2 + 1)\ CCF, \qquad (3)$$

where P_1 and P_2 are the non-recurring fabrication/assembly engineering and materials cost factors, respectively. CCF is the fabrication or assembly complexity factor. The function F(V) is defined as:

$$F(V) = PHI\,(V)^{-k}, \qquad (4)$$

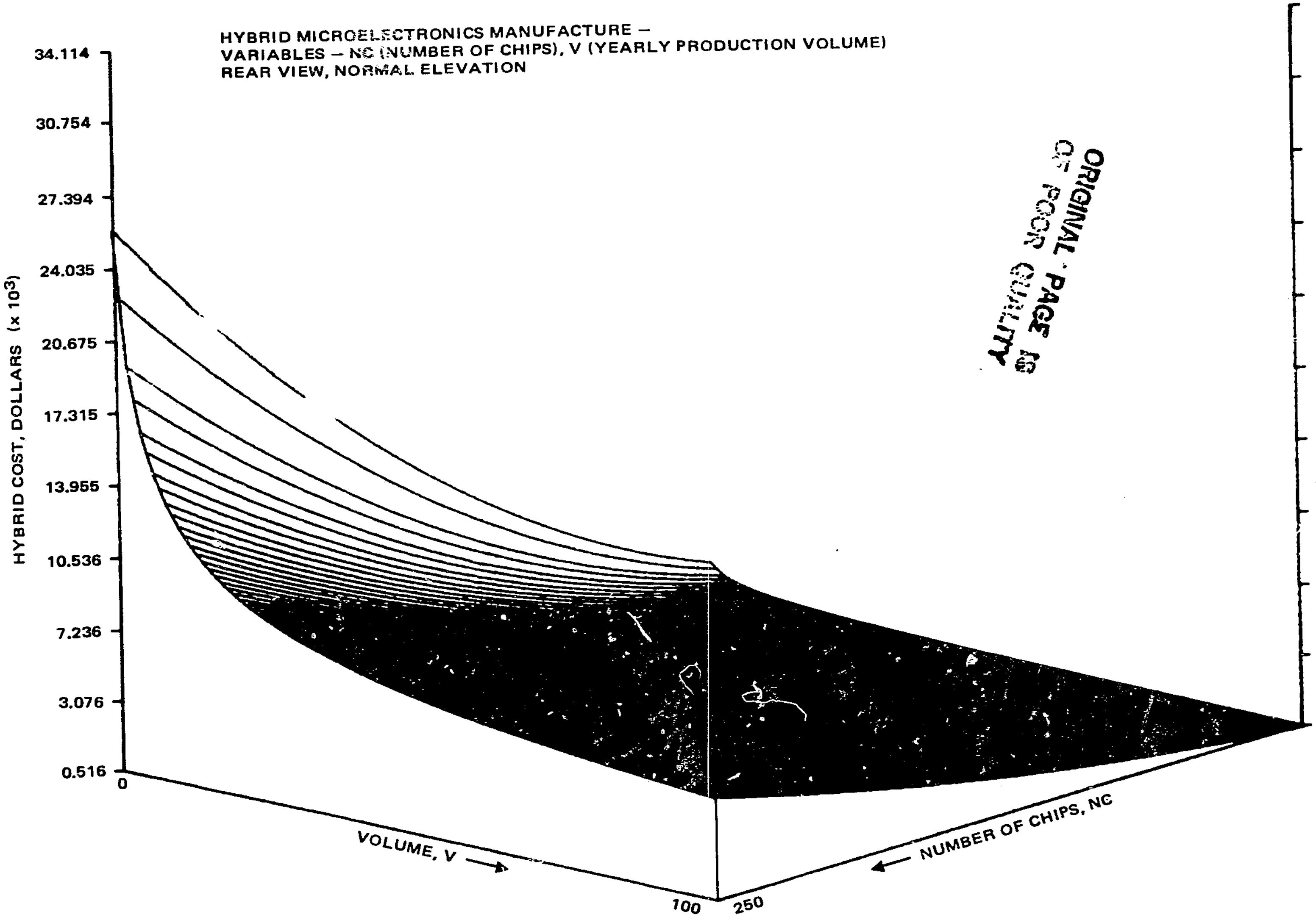


Figure 2-5. Total hybrid cost as a function of total number of drips and production volume (rear view).

where PHI depends upon the type of production facility chosen (prototype or large volume), and k is a constant representing the slope of the log-log plot in Figure 2-6. The two straight lines in this figure represent two different types of production facilities, and intersections with the cost axis determine values of PHI.

Non-recurring costs were introduced into the manufacturing cost equation for the purpose of generating general equations, from which special cases can be obtained. In fact, by making $P_1 = P_2 = 0$, one can separate the non-recurring cost from total manufacturing cost.

2.1.2.1 Non-Recurring and Recurring Materials Costs (Conventional (PWB) Packaging)

Non-recurring cost factors were collected for conventional packaging via PWB fabrication and assembly. These costs were divided into two categories:

1. Engineering - including design, design review, implementation, initial planning, test procedures, preparation of specification, and layout;
2. Materials - including fixtures and tooling, artwork, drill tape, computer program for breadboard testing, and various assembly aids.

These costs are included in Tables 2-1 and 2-2 respectively.

The recurring material costs also were collected for PWB fabrication, and for conventional (PWB) assembly; they are reported in Table 2-3. Recurring fabrication costs include the cost of board material, (glass polymide and/or glass epoxy), prepregs used for lamination in multilayer fabrication, chemicals (photoresist, stripper, etchants, cleaner, electroplating baths), and gold electroplating solution. Recurring assembly costs include the cost of component parts such as resistors (passive axial components in general), diodes, transistors, hybrid microcircuits, and flat packs. These costs are expressed explicitly in dollars, whereas the non-recurring fabrication and assembly costs are expressed as percentages of PWB fabrication and assembly costs, respectively.

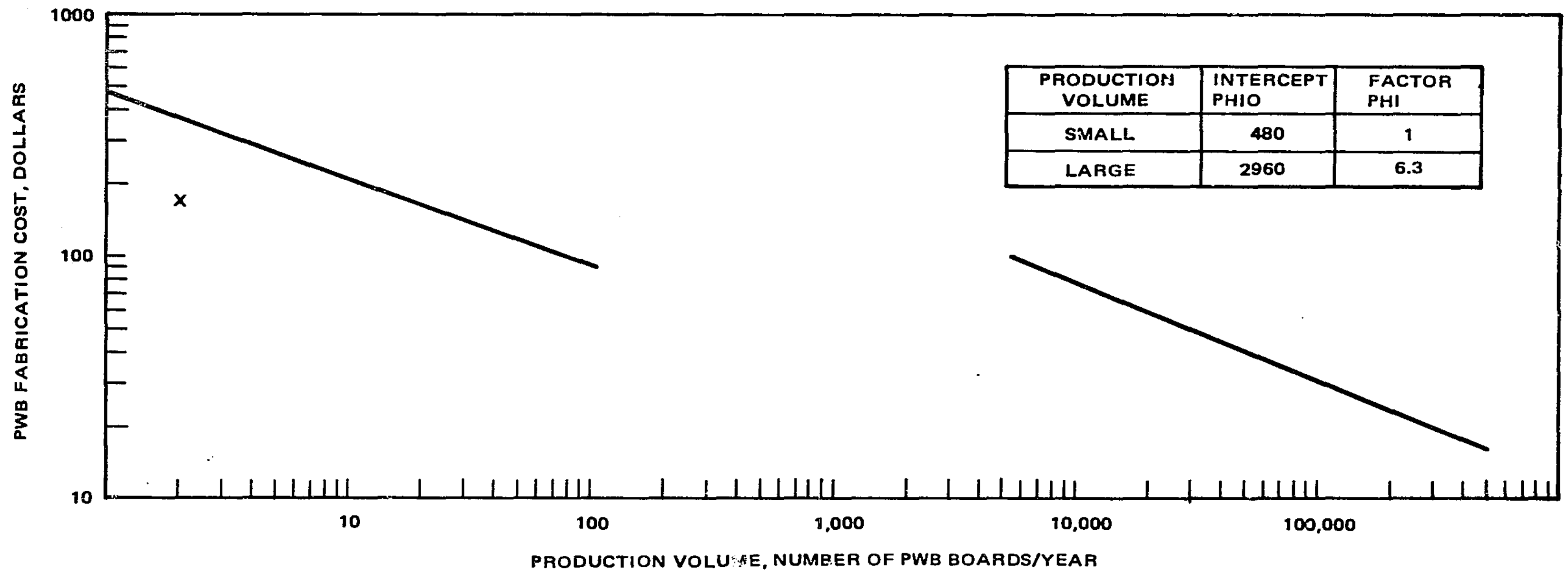


Figure 2-6. PWB fabrication cost as function of production volume per different types of facilities.

TABLE 2-1. NON-RECURRING PWB FABRICATION COSTS (P_{1F}, P_{2F})

Cost Category	Cost Breakdown		Percentage of Total Fabrication Cost
Engineering, P_{1F}	Design, design review	25%	20 - 30%
	Implementation support	10%	
	Initial planning	15%	
	Preparation of specifications, test procedures	25%	
	Layout	25%	
Materials, P_{2F}	Fixture and tooling	30%	20 - 25%
	Artwork	35%	
	Drill tape	15%	
	Computer program for breadboard testing	20%	

TABLE 2-2. NON-RECURRING CONVENTIONAL PACKAGING (PWB) ASSEMBLY COSTS (P_{1A}, P_{2A})

Cost Category	Cost Breakdown		Percentage of Total Assembly Cost
Engineering, P_{1A}	Design, design review	25%	20%
	Initial planning	15%	
	Implementation support	20%	
	Preparation of specifications, test procedures	15%	
	Layout	25%	
Materials, P_{2A}	Fixture, tooling, assembly aids		30 - 35%

TABLE 2-3. RECURRING MATERIAL COSTS (CMRF)

PWB Fabrication
1. Board material: glass-polyimide or glass-epoxy with copper cladding
2. Lamination material: polyimide or epoxy prepreg
3. Chemicals: photoresist, etchants, electroplating baths, solder, stripper, cleaner, brightener
4. Gold bath
PWB Assembly
1. Axial components (resistors, capacitors)
2. Transistors
3. Flat packs (mainly used with digital modules)
4. Hybrids

Mathematically, the non-recurring costs may be expressed by an equation of the type

$$P_F = (P_{1F} + P_{2F})\ \mathrm{CCFAB} \tag{5}$$

for PWB fabrication, and by a similar equation

$$P_A = (P_{1A} + P_{2A})\ \mathrm{CCA} \tag{6}$$

for PWB assembly. CCFAB and CCA are complexity factors of PWB fabrication and assembly respectively.

Fabrication recurring costs (CMRF) can be modeled by the equation:

$$\mathrm{CMRF} = \mathrm{CMM} + \mathrm{CMP} + \mathrm{CCH} + \mathrm{CAU} \tag{7}$$

where

$CMM = 2 \cdot F \cdot NL \cdot SF$	Board Materials Cost
$CMP = 0.36 \cdot F \cdot NL \cdot SF$	Prepreg Cost
$CCH = 0.8$	Cost of Chemicals
$CAU = 2.5$	Cost of Gold Bath

Assembly recurring cost (CMRA) is modeled by the equation:

$$CMRA = CCOMP + COO , \tag{8}$$

where COO is a constant which accounts for minor miscellaneous materials costs, and the "component parts cost" term CCOMP for analog circuit applications is given by:

$$CCOMP = 0.52 \cdot NAX + 3.5 \cdot NTR + 450 \cdot NHY \tag{9}$$

For digital circuit applications, the component parts cost is:

$$CCOMP = 1.5 \cdot NFP , \tag{10}$$

where NFP is the number of flat-packs (or DIPs). (Definition of terms is included in Table 2-4). The numbers in these equations are the average unit component parts costs in dollars.

2.1.2.2 Printed Wiring Board (PWB) Fabrication

To formulate the model for PWB fabrication to be used in conventional electronics packaging/assembly, it was necessary to a) collect quantitative cost factors, and b) model each step of the process. Qualitative cost factors already have been collected in previous work[1].

1. Quantitative Cost Factors Collection

   Costs were associated with each of the major steps necessary to fabricate a PWB. This was achieved by examining several work sheets collected from different production facilities. Each of these costs was expressed further in terms of process parameters. As a consequence, pairs of parameters, such as cost of fabrication and number of layers (Figure 2-7), cost of fabrication and yearly quantity produced (Figure 2-6), and cost of fabrication and weight of the copper-clad material (Figure 2-8), have been related and expressed in graphical form.

TABLE 2-4. DEFINITION OF TERMS: PWB FABRICATION

CLEAN = 0.5	Cleaning factor	1 good 0.5 satisfactory 0.25 poor
CMF = 1	Complexity of masking operation	1.5 extensive 1.0 normal
CPB = 0.015	Post-bake cost	
HD = 25	Hole density	
HDS = 3	Number of different hole sizes	
HN = 800	Number of holes	
HS = 32	Hole size	
LS = 10	Line spacing	
LW = 12	Line width	
NI = 10	Number of inspections	
NL = 6	Number of layers	
A = 0.37	CARRIER coefficient	
NL = 6 A	CARRIER case only	
NRETC = 3	Number of retouchings, copper	
NRHPL = 1	Number of replatings	
NRPHR = 5	Number of photoresist retouchings	
NT = 59	Number of terminals	
PS = 40	Pad size	

(Continued next page)

Table 2.4, (concluded)

PSF = 1	Press cycle factor	1 epoxy 1.5 polyimide
PWBA = 30	PWB area, square inches	
QHF = 0.5	Hole quality factor	1 smooth 0.5 medium 0.3 rough
QPLF = 0.5	Plating quality factor	1 good 0.5 satisfactory 0.25 poor
TAHF = 1	Adhesive type	1 prepreg 1.5 polysulfone
TCC = 1	Curing cycle	1 epoxy 2.5 polyimide
TCUF = 0.0175	Copper thickness factor, STDH/ounce	
THSF = 1	Type of heat sink	1 normal 1.5 complex
TMAR = 1	Type of marking	1.5 stencil 1.0 etched
TMF = 1	Type of material	1 epoxy 1.8 polyimide
TR = 0.05	Drilling tolerance	
TYR = 0.5	Type of photoresist	0.3 self-screening 0.5 film resist 1.0 liquid
WCU = 2	Weight of copper, ounces	
X = 0.23	Drilling tolerance (TR) exponent	
SF = 0.5	Size factor	0.3 size 2 in. x 3 in. 0.5 size 5 in. x 6 in. 1.0 size 8 in. x 12 in.

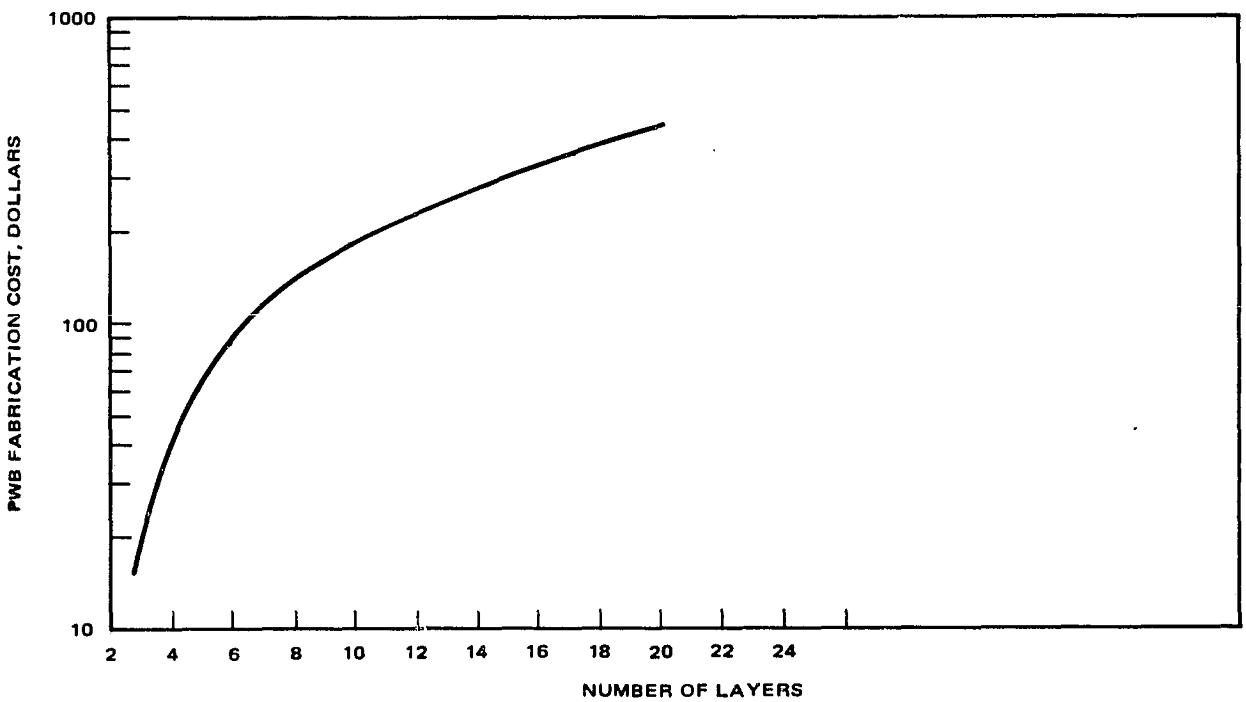


Figure 2-7. Printed wiring board (PWB) fabrication cost as a function of the number of board layers.

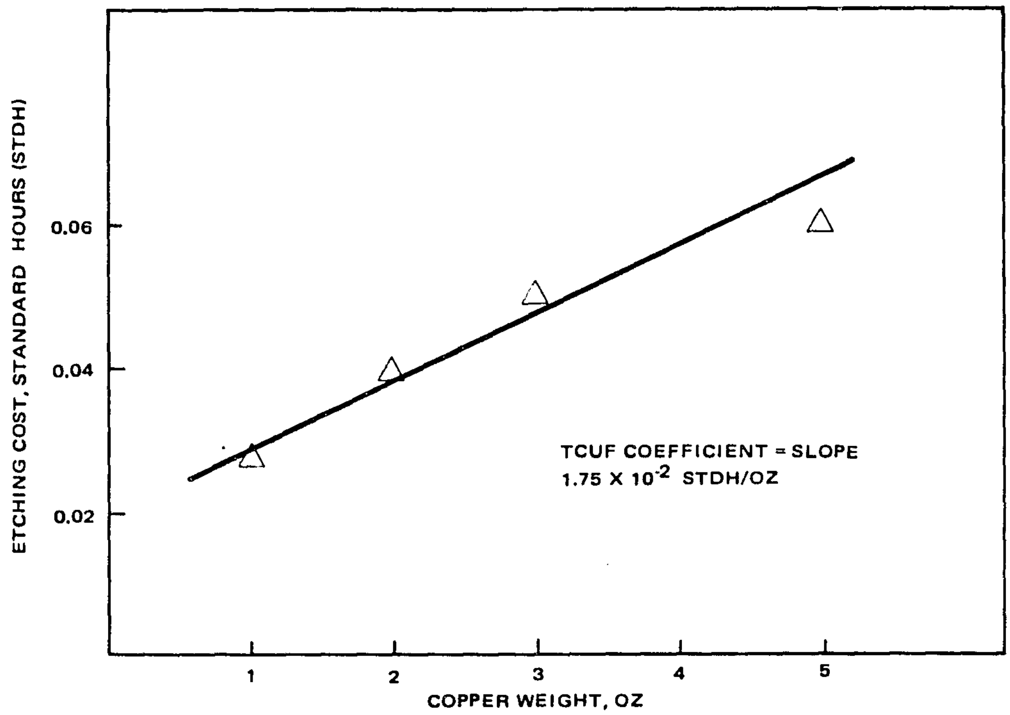


Figure 2-8. Etching cost as a function of PWB copper weight.

2. Process Modeling

Process parameters and time of fabrication were related for each step of the fabrication process, which was simplified to include only important steps. The fabrication process has been modeled by the flow chart in Figure 2-9.

At first, a functional relationship between these quantities was established. Then, the constants of proportionality were derived by applying values as they relate to quantities, process parameters, and costs in standard hours, previously collected.

A complexity factor has been defined as a function of hole density, line width, line spacing, pad size, hole size, and number of layers. The PWB fabrication cost then was expressed by an equation which is the sum of each single process step cost, including the complexity factor.

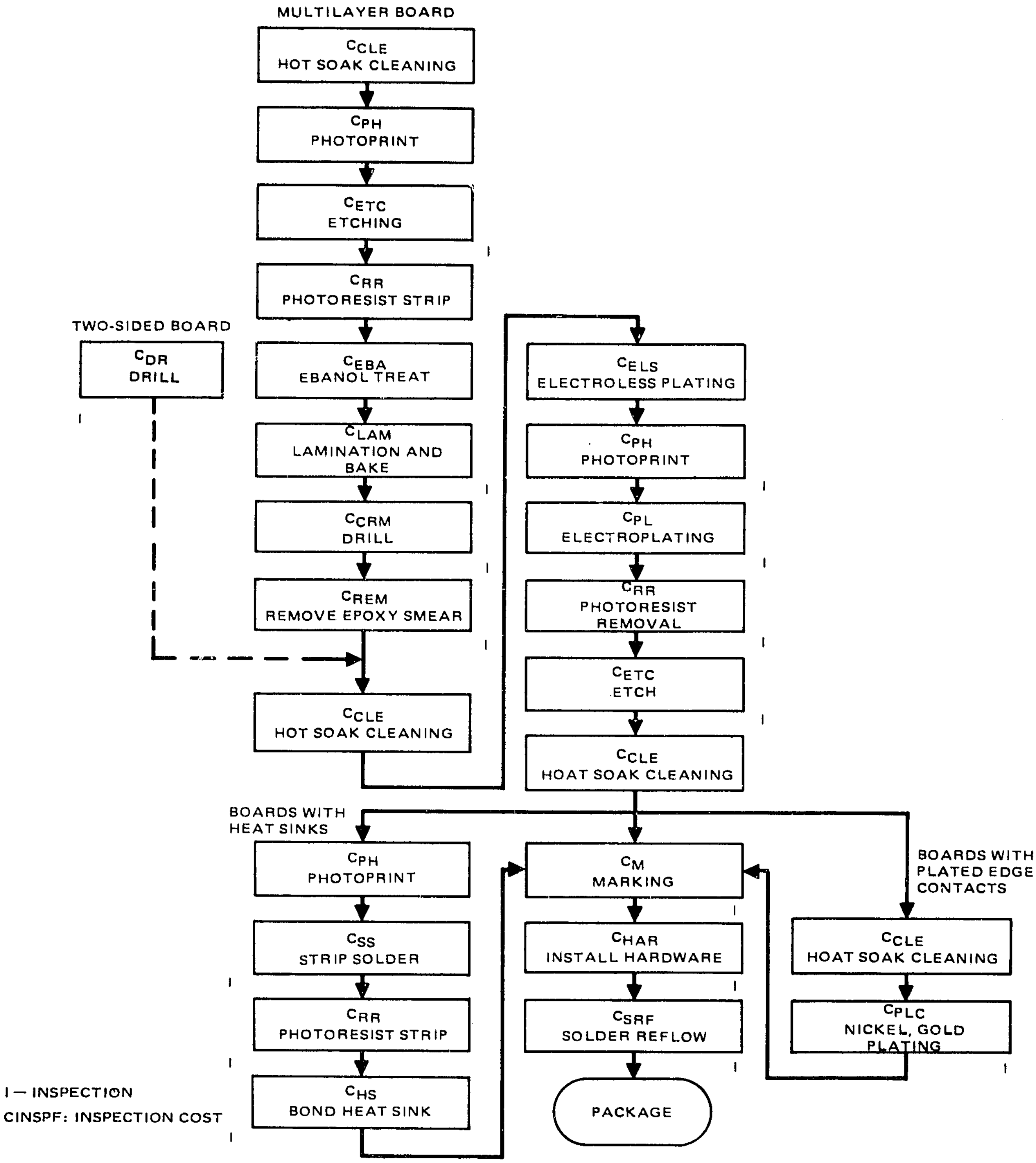


Figure 2-9. Printed wiring board processing sequence.

2.1.2.2.1 Mathematical Formulation of the Model

The cost in dollars of conventional (PWB) fabrication (CPMFAB) has been modeled by the following equation:

$$CPMFAB = CMFAB\,(PF1 + PF2 + 1)\,CCFAB \cdot PHI\,(V)^{-K}, \qquad (11)$$

where CMFAB is the volume-and-non-recurring- cost-independent expression of conventional (PWB) fabrication cost. CMFAB is given by

$$\begin{aligned} CMFAB = (&CCL + CPH + CETC + CCR + CEBA + CLAM \\ &+ CDRM + CREM + CELS + CPL + CM + CHAR \\ &+ CSRF + CPLC + CHS + CINSPF + CETF \\ &+ CRWF) \cdot WR\,, \end{aligned} \qquad (12)$$

where WR is the wage rate, and all other symbols are identified by steps in the flow chart of Figure 2-9.

The above equation is based on relationships between process step cost and process parameters, as indicated in Table 2-5.

The numbers appearing in the equations are the constants of proportionality. These constants were obtained by giving average values to the process parameters once the process step cost was known. Symbols expressing the process parameters, their meanings, and their typical numerical values, are listed in Table 2-4.

The complexity factor CCFAB is defined as

$$\begin{aligned} CCFAB &= (2.1 \times 10^{-3} \cdot HD + 0.67 \cdot (1./LW + 1./LS))^{ALPHA} \\ &= 5 \cdot (1/PS)^{BETA} + 4 \cdot (1/HS)^{GAMMA} \\ &\quad + 0.0125 \cdot (NL)^{DELTA} \end{aligned} \qquad (13)$$

where alpha, beta, gamma, and delta are exponents chosen to be numerically equal to one. This relationship was found empirically to be the most suitable for applications under this program. Further refinement of this equation might be obtained by giving more weight to some of these exponents than to others. The numerical values of the four exponents however, should remain close to unity.

TABLE 2-5. PWB FABRICATION PROCESS PARAMETERS

Hot soak cleaning	$CCLE = 0.0133 \bullet NL$
Photoprinting	$CPH = 0.16 \bullet TYR \bullet SF \bullet NL$
Etching	$CETC = CCFAB \bullet 0.86 \bullet NL \bullet TCUF \bullet WCU$
Photoresist stripping	$CRR = 5.5 \times 10^{-3} \bullet NL \bullet CCFAB$
Ebanol treatment	$CEBA = 4.2 \times 10^{-3} \bullet NL$
Lamination and bake	$CLAM = 2.5 \times 10^{-2} \bullet NL \bullet TMF \bullet PSF \bullet CPB$
Drilling	$CDRM = (3.4 \times 10^{-4} \bullet HN + 0.09 \bullet HDS) \bullet (TR)^{x} \bullet QHF$
Removal of epoxy smear	$CREM = 0.062 \bullet TMF \bullet QHF \bullet TCC$
Electroless plating	$CELS = (6.25 \times 10^{-3} \bullet HS + 0.008 \bullet HD) \bullet CLEAN$
Electroplating	$CPL = 0.0111 \bullet CCFAB \bullet HS$
Marking	$CM = 0.006 \bullet TMAR$
Installation of hardware	$CHAR = 48 \times 10^{-3} \bullet NT \bullet CCFAB$
Solder reflowing	$CSRF = 0.226 \bullet QPLF$
Ni and Au plating	$CPLC = 0.9 \bullet SF \bullet CCFAB \bullet CMF$
Bond heat sink	$CHS = 0.15 \bullet THSF \bullet TAHF$
Inspection	$CINSPF = 8.8 \times 10^{-3} \bullet CCFAB \bullet SF \bullet NI$
Electrical testing	$CETF = 1.2 \bullet CCFAB \bullet SF$
Rework	$CRWF = 0.055 \bullet NRETC + 0.166 \bullet NRHPL + 0.0333 \bullet NRPHR$

2.1.2.3 Conventional PWB Assembly

The assembly model for conventional (PWB) electronics subsystem packaging was formulated in a manner similar to that used for PWB fabrication. Three steps were followed:

1. Collection of Quantitative Cost Factors

   A cost figure was given to each major step of the assembly process. These cost figures were obtained from different production facilities involved in either manual or automatic assembly of discrete capacitors and/or other component parts on a PWB board. Quantitative values for parameters such as rate of component lead forming, rate of component insertion, rate of magazine loading, rate of leak test, rate of timing, and rate of vapor cleaning, also were collected. In addition, average values have been determined for a typical assembly sequence, and a reference set of PWB assembly costs has been established.

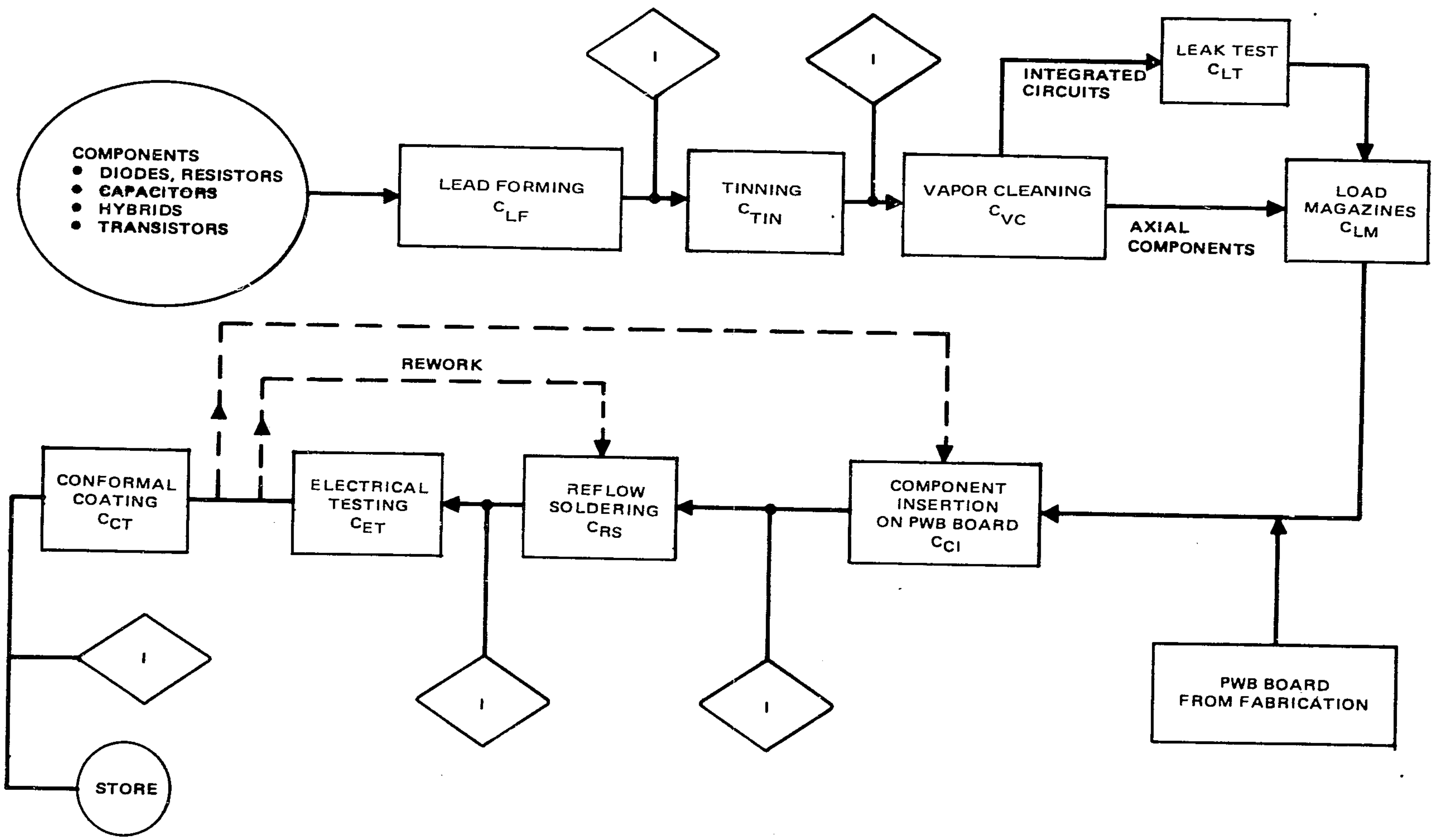
2. Modeling

   Process parameter costs were related by functional mathematical relationships for each step of the assembly process (Figure 2-10); simplified to include only important steps. Once the shape of the functions was established, the constants of proportionality were determined by using the quantitative values previously collected. In this case also, as was done for the PWB fabrication model, a complexity factor has been defined. The assembly complexity factor was found to be a function of the density of axial-leaded component parts, the density of other component parts (including transistors and hybrid microcircuits for analog subsystems, or flat packs for digital subsystems), and the average component lead density. Further, this complexity factor was defined to be numerically equal to the PWB fabrication complexity factor for any given set of parameters. The PWB assembly cost then was expressed by an equation involving the sum of each process step cost, and including the complexity factor.

3. Mathematical Formulation of the Model

   The cost in dollars for the assembly of discrete electronic component parts on a PWB is modeled by the following equation:

$$[illegible]A = CMA \cdot (PA1 + PA2 + 1) \cdot PHI\,(V)^{-K} \cdot CCA\,, \qquad (14)$$



I = INSPECTION

Figure 2-10. Printed wiring board assembly process for surface mounted component parts.

where CMA is the volume-and-non-recurring-cost-independent PWB assembly and testing cost. CMA is given by:

$$\mathrm{CMA} = (\mathrm{CLF} + \mathrm{CTIN} + \mathrm{CVC} + \mathrm{CLT} + \mathrm{CLM} + \mathrm{CCI} + \mathrm{CRS} + \mathrm{CETA} + \mathrm{CTROB} + \mathrm{CRWA} + \mathrm{CCT} + \mathrm{CINSPA}) \cdot \mathrm{WR}\ , \quad (15)$$

where WR is the wage rate, and all other symbols are identified through the flow chart steps shown in Figure 2-10.

Each step of equation (15) is based upon relationships between those process step costs and process parameters shown in Table 2-6.

Numbers included in the equations (and in Table 2-6) are constants of proportionality. These constants were determined by giving representative values to the process parameters, once the process step cost was known. The meaning of the symbols expressing the process parameters and their typical numerical values are listed in Table 2-7.

The assembly complexity factor CCA is defined as:

$$\mathrm{CCA} = \mathrm{CA1} \cdot (\mathrm{DAX} + \mathrm{DOT}) + \mathrm{CA2}(\mathrm{DLAB})^{1.1}\ , \quad (16)$$

where the exponent 1.1 has been chosen empirically to fit the experimental data. The shape of this equation also has been determined empirically by means of a trial-feedback approach.

2.1.3 Hermetic Chip Carriers - Introducing a New Technology into a Well-Established Technology

The introduction of new technologies into traditional production lines can be expensive, if all major consequences are not properly determined. Predictions concerning these consequences can be made effectively by employing modeling techniques.

The hermetic chip carrier (HCC) (shown in Figure 2-11) is a fast-developing technology which has found applications on printed wiring boards (PWBs) and on ceramic wiring boards (CWBs) as a direct replacement for flat packs or dual-in-line-packaged (DIP) components. Preliminary cost analyses show that hermetic chip carriers (generally fabricated from ceramic for military-grade applications; or from either plastic or ceramic for commercial applications) are an economical method of packaging LSI chips.

TABLE 2-6. PWB ASSEMBLY OF COMPONENT PARTS - PROCESS PARAMETERS

Lead forming	$CLF = NA \cdot 0.075 (NAX/RFORA + NTR/RFORT + NHY/RFORH) \cdot BF$
Tinning	$CTIN = NA \cdot 0.06 \cdot NC/RTIN$
Vapor cleaning	$CVC = NA \cdot 0.055 \cdot NC/RVC$
Leak test	$CLT = NA \cdot R \cdot 0.065 \cdot NC/RLT$
Load magazines	$CLM = NA \cdot 0.3 \cdot NC/RLM$
Component insertion	$CCI = NA \cdot 0.15 \cdot (NAX/RIA + NTR/RIT + NHY/RIH) \cdot BF$ ($CCI = (NFP/RIFP \cdot BF$ for digital systems)
Reflow soldering	$CRS = 0.03$
Electrical testing	$CETA = 0.88 (AVCCC)^{Y} \cdot CCA$
Troubleshooting	$CTROB = 2.2 (AVCCC)^{Y} \cdot CCA$
Rework	$CRWA = N (0.175 \cdot N1 \cdot NHY + 0.054 \cdot N2 \cdot NOTH + 0.011 \cdot N3 \cdot NSJ)$
Conformal coating	$CCT = 0.15 \cdot SF$
Inspection	$CINSPA = NI \cdot 0.088 \cdot CCA \cdot SF$

TABLE 2-7. DEFINITION OF TERMS: CONVENTIONAL (PWB) PACKAGING ASSEMBLY (RATES ARE EXPRESSED IN NUMBERS OF COMPONENT PARTS/HOUR)

AVCCC = 0.5	Average component complexity factor
BF = 1	Bending factor (1= automated; 10 = manual
CA1 = 0.056	Assembly complexity factors constant
CA2 = 0.009	Assembly complexity factors constant
DAX = NAX/PWBA,	Axial component density
DLAV = 26	Average lead density per component
DOT = NOTH/PWBA,	Other component density
N = 1	Number of reworks
N1 = 0.1	Fraction of hybrids reworked
N2 = 0.02	Fraction of other components reworked
N3 = 0.01	Fraction of solder joints
NA = 2	Number of sides
NAX = 80	Number of axial components
NC = 94	Number of components
NFP = 94	Number of flat packs
NHY = 10	Number of hybrids
NI = 5	Number of inspections
NOTH = 14	Number of other components
NSJ = 800	Number of solder joints
NTR = 4	Number of transistors
R = 1	Component type (1 = axial; 0 = other)
RFORA = 60	Rate of forming of axial components
RFORFP = 1200	Rate of forming of flat packs
RFORH = 120	Rate of forming of hybrids
RFORT = 20	Rate of forming of transistors
RIA = 60	Rate of insertion of axial comps.
RIFP = 1200	Rate of insertion of flat packs
RIH = 120	Rate of insertion of hybrids
RIT = 20	Rate of insertion of transistors
RLM = 500	Rate of loading
RLT = 50	Rate of leak test
RTIN = 50	Rate of tinning
RVC = 100	Rate of vapor cleaning
Y = 1	Exponent of AVCCC
PWBA = 30 in^2	Area of board

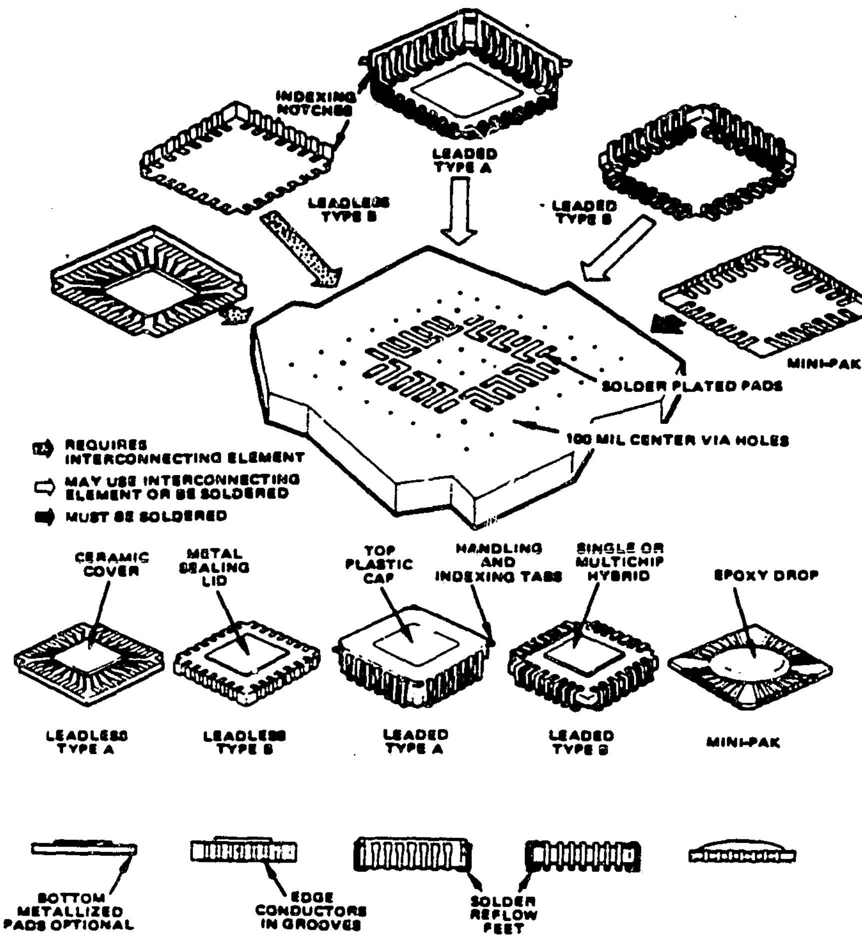


Figure 2-11. Hermetic chip carrier configurations.

In view of the performance improvements and size/weight reductions associated with HCC technology, it is important to determine the cost effects of these packages on conventional PWB electronics subsystem fabrication when the two technologies are combined.

Cost factors related to HCC technology were collected from an internal study intended to modify some of the actual electronic modules for the F-15 Radar System[3]. By constructing a selected PWB module (originally designed with through-holes to permit usage of wave-soldered flat-packs) utilizing the same number of surface-reflow-soldered HCC packages, cost savings can be realized in fabricating the board by laminating five layers, instead of the eight layers which otherwise would be required. This reduction in the number of layers can be expressed as a space savings of about 44 percent. Savings also are achieved in the HCC package assembly process. The difference between HCC and flat-pack assembly processes is represented in Figure 2-12. Additional handling, lead forming, and lead cutting steps are needed to assemble flat-packs, while the cost of assembling LSI chips into HCC packages is about the same as that for chips mounted in flat-packs. This process can be modeled in both cases (flat-packs and HCC packages) by means of the flow charts shown in Figure 2-13.

The assembly of hermetic chip carriers onto PWBs was modeled from the process represented in Figure 2-14. An analysis of this simplified process shows that the cost of HCC assembly is modeled by the equation

$$CMA = ((CLF+CTIN+CVC+CLT+CLM+CCI+CRS+CETA+CTROB +CRWA+CCT+CINSPA)\cdot(1+D) - (CLF+CTIN+CLT))\cdot WR, \quad (17)$$

where D is a factor representing the assembly cost differential when HCCs are used. Other cost savings are associated with materials costs. Hermetic chip carriers can be purchased at a lower unit price than can flat-packs. The difference in cost of these units as a function of lead/pad count is reported in Figure 2-15.

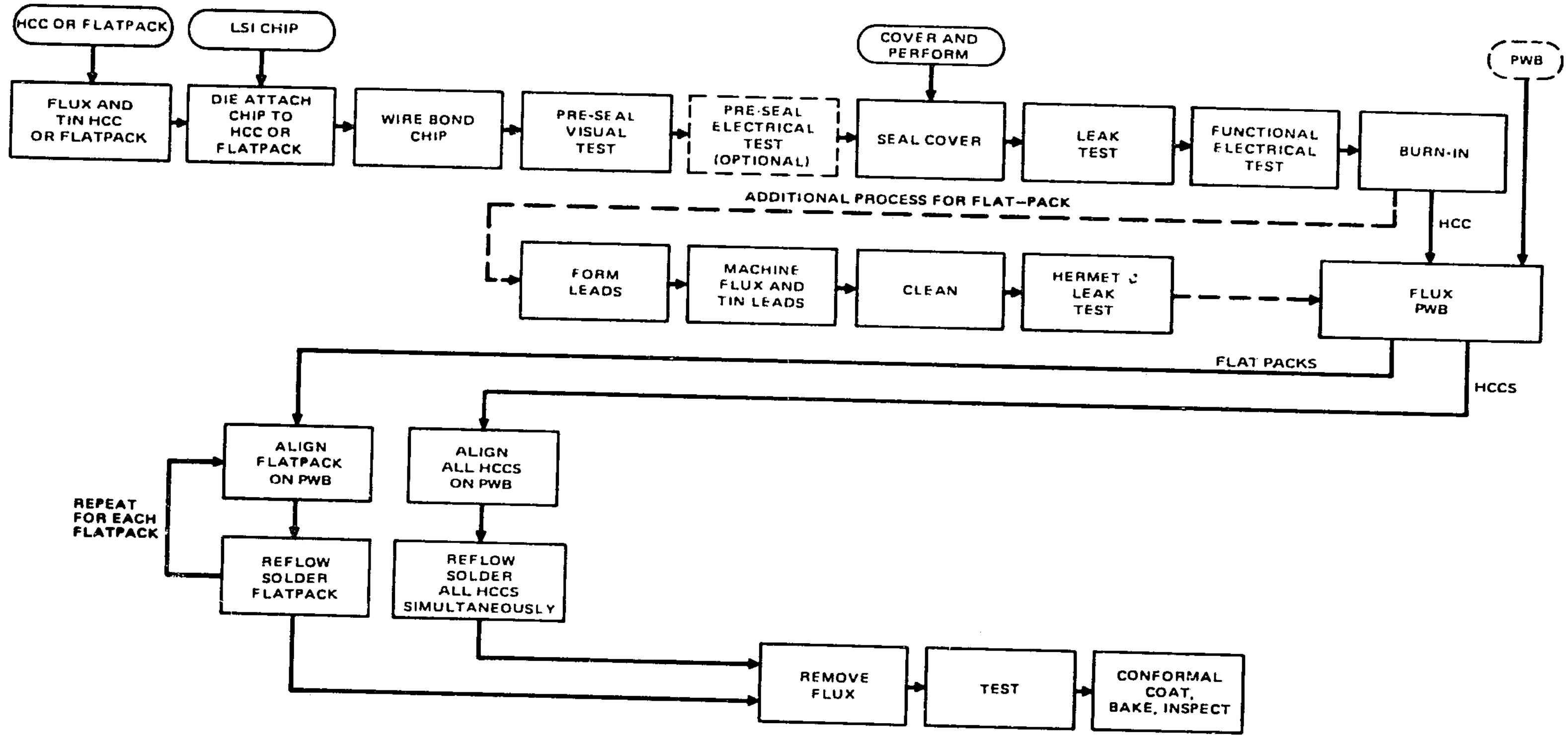
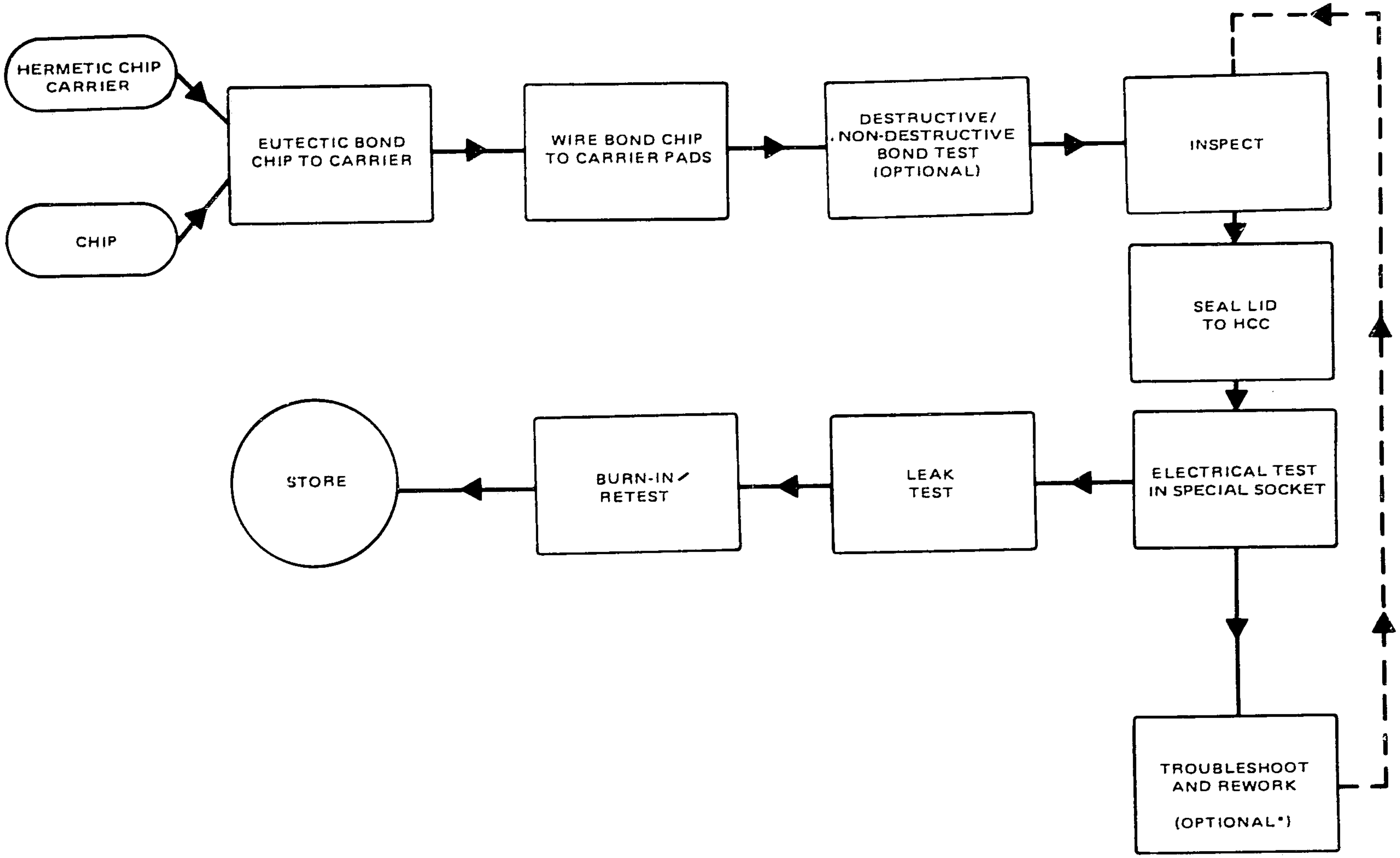


Figure 2-12. Comparison between hermetic chip carrier (HCC) and flatpack processes.



*GENERALLY NOT PRACTICAL FOR HCC PACKAGES

Figure 2-13. Assembly of a chip into a hermetic chip carrier.

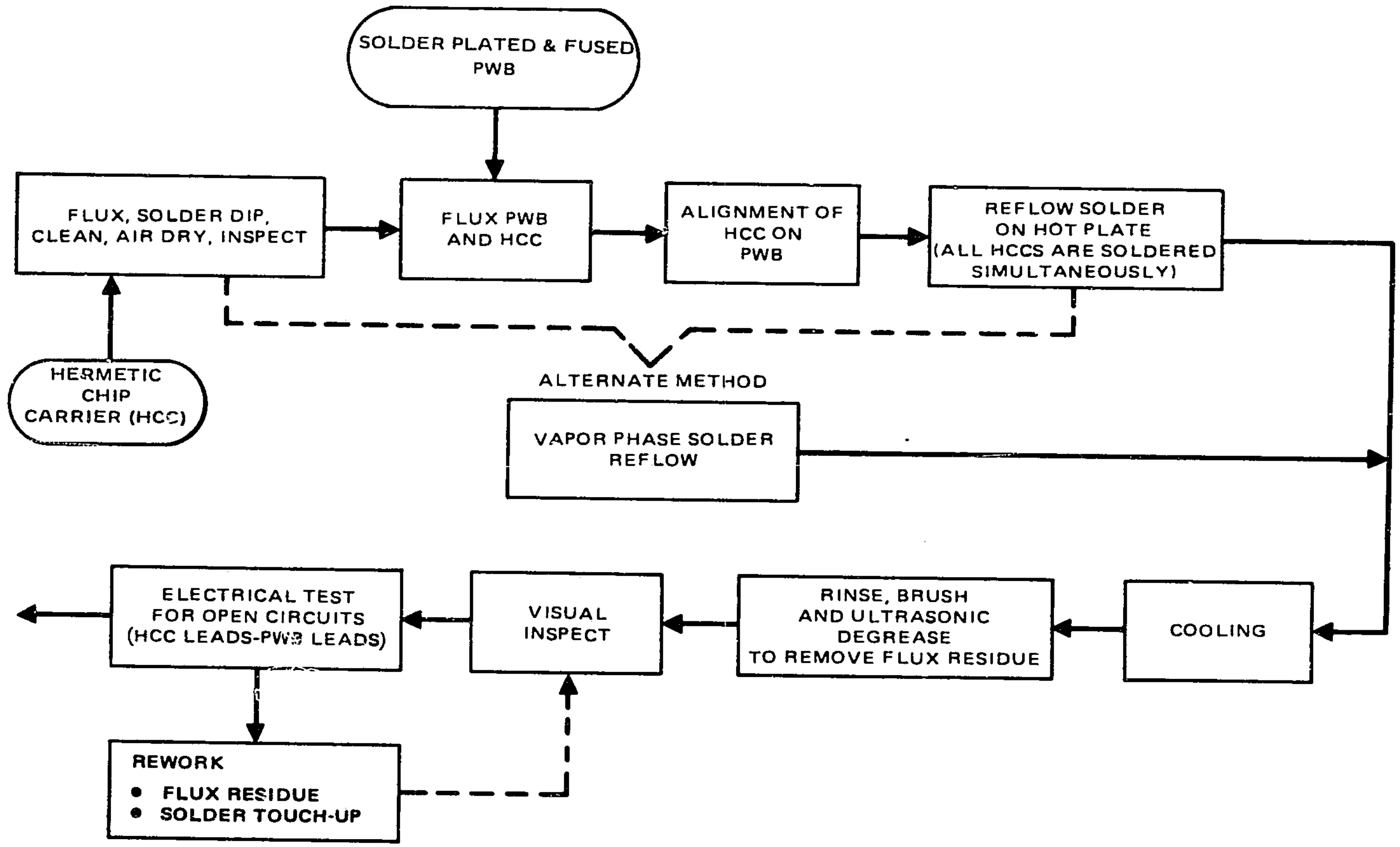


Figure 2-14. Hermetic chip carrier (HCC) assembly onto printed wiring board (PWB).

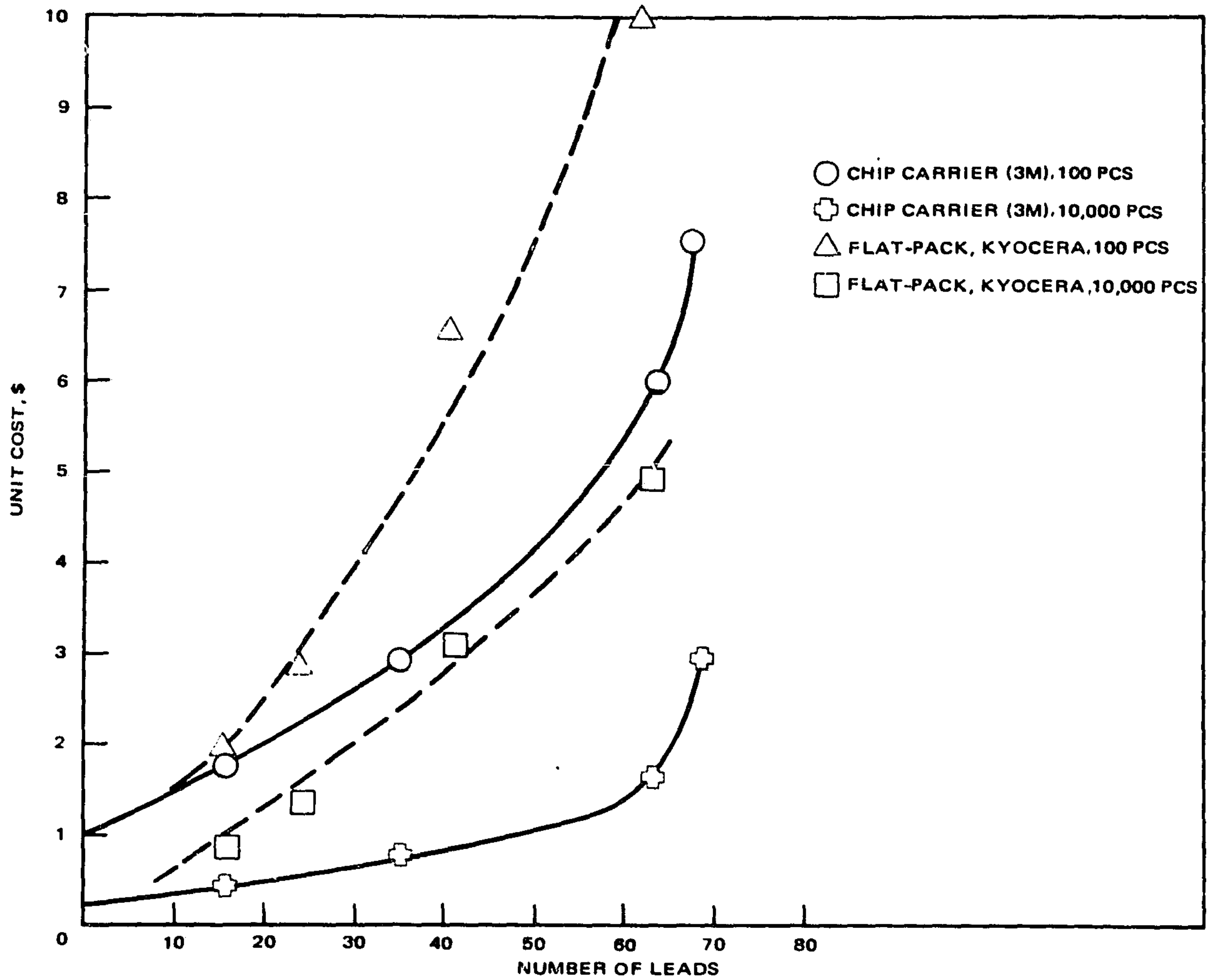


Figure 2-15. Hermetic chip carrier cost vs numbers of leads/pads.

The component parts material cost, (CCOMP) then is modified to include the cost effects of the HCC package:

$$CCOMP = B \cdot 15 \cdot NFP \, , \tag{18}$$

where B is a coefficient of proportionality. The term $B \cdot NFP$ is the actual number of HCC packages used. The number 15 represents an average cost value for flat-packs with LSI chips, and NFP is the number of flat-packs.

In addition to the above-described cost savings when HCC packages are utilized, the cost of associated materials items such as CMM and CMP (page 2-14) is reduced because of the space savings attained with HCCs.

2.1.4 Computer Programming and Models Verification

Computer programs were developed for the computation of PWB manufacturing costs in a fashion similar to that developed for hybrid microelectronics subsystems. Such models, developed and expressed with mathematical equations, turned out to be equally suitable for programming, when compared with the hybrid models. Consequently, the computer was used not only to verify the initial functional relationships assumed to exist between parameters and costs, but also to refine them.

Two computer programs were written: one to compute a single-valued cost function; the other, to generate a cost surface. The single-valued-cost-function program includes three application cases: analog, digital, and hermetic chip carrier. Normally, the program computes the cost for the analog case if the other two are not requested specifically.

Hermetic chip carrier technology is a growing LSI packaging approach which allows dense packaging of LSI chips, along with improved performance. A cost impact study in comparison with more traditional technologies (such as conventional PWB assembly) is important as an aid to enhanced implementation of this relatively new technology into the mainstream of electronics packaging methodology. The cost factors and equations developed for the HCC technology were computerized, and the total cost of PWB manufacture/assembly with HCC packages was computed.

For a given set of input variables, the program computes and prints out PWB fabrication cost, PWB assembly cost, recurring material fabrication cost, recurring material assembly cost, fabrication complexity factor, assembly complexity factor, and total manufacturing PWB cost for the three cases (analog, digital, and PWB module with HCC packages).

The program to compute a single-valued function is reported in Appendix D; typical print-outs are shown in Figure 2-16. Meanings of the symbols used, and that of the process steps have been included in the program printout, so that interpretation of the equations is relatively simple.

The computer programs required to generate cost surfaces were developed for conventional (PWB) fabrication/assembly in a manner similar to that utilized for hybrid microelectronics. This program, shown in Appendix E, generates a matrix of cost values which then are plotted by means of any convenient graphical display program to generate cost surfaces.

A typical graphical output computed from usage of this program is shown in Figure 2-17, which illustrates the total manufacturing cost surface as a function of layers and production volume. An alternate view of this same cost surface is obtained by rotating the axes, as shown in Figure 2-18. As production volume decreases and the number of layers increases, the cost increases. The non-linear behavior of cost with these parameters is attributable largely to the presence of the production-volume term.

When the cost surface representing total PWB manufacture and assembly is compared to that for PWB fabrication alone (represented in Figure 2-19), it can be seen that the latter varies with the number of layers (especially at low production volume) much more than does the total PWB manufacturing/assembly cost. Evidently those costs involved in the assembly of conventional component parts onto PWBs cause potentially significant changes in the overall surface shape.

2.1.5 Recommendations for Future Study (Task A)

Mathematical cost models are useful only if they can be interpreted easily by engineers, designers, and production managers to estimate the cost evolution of electronic systems as the technology changes. Model representation therefore must be easy to understand, and the means for

PRINTED WIRING BOARD MANUFACTURE:

SPECIAL CASE SELECTED: NONE (NONE = ANALOG)
(CARRI = CARRIER; DIGIT = DIGITAL)

PWB FABRICATION COST C'MFAB = $214.54
PWB ASSEMBLY COST C'MA = $236.10

RECURRING MATERIAL FABRICATION COSTS CMRF = $10.38
RECURRING MATERIAL ASSEMBLY COSTS CMRA = $4575.60

FABRICATION COMPLEXITY FACTOR CCFAB = .500
ASSEMBLY COMPLEXITY FACTOR CCA = .500

TOTAL MANUFACTURING COST CPWB = $5036.61

PRINTED WIRING BOARD MANUFACTURE:

SPECIAL CASE SELECTED: CARRI
(CARRI = CARRIER; DIGIT = DIGITAL)

PWB FABRICATION COST C'MFAB = $159.64
PWB ASSEMBLY COST C'MA = $338.50

RECURRING MATERIAL FABRICATION COSTS CMRF = $5.92
RECURRING MATERIAL ASSEMBLY COSTS CMRA = $823.70

FABRICATION COMPLEXITY FACTOR CCFAB = .453
ASSEMBLY COMPLEXITY FACTOR CCA = .500

TOTAL MANUFACTURING COST CPWB = $1327.77

PRINTED WIRING BOARD MANUFACTURE:

SPECIAL CASE SELECTED: DIGIT
(CARRI = CARRIER; DIGIT = DIGITAL)

PWB FABRICATION COST C'MFAB = $214.54
PWB ASSEMBLY COST C'MA = $185.73

RECURRING MATERIAL FABRICATION COSTS CMRF = $10.38
RECURRING MATERIAL ASSEMBLY COSTS CMRA = $1430.00

FABRICATION COMPLEXITY FACTOR CCFAB = .500
ASSEMBLY COMPLEXITY FACTOR CCA = .500

TOTAL MANUFACTURING COST CPWB = $1840.65

Figure 2-16. Typical PWB print-outs.

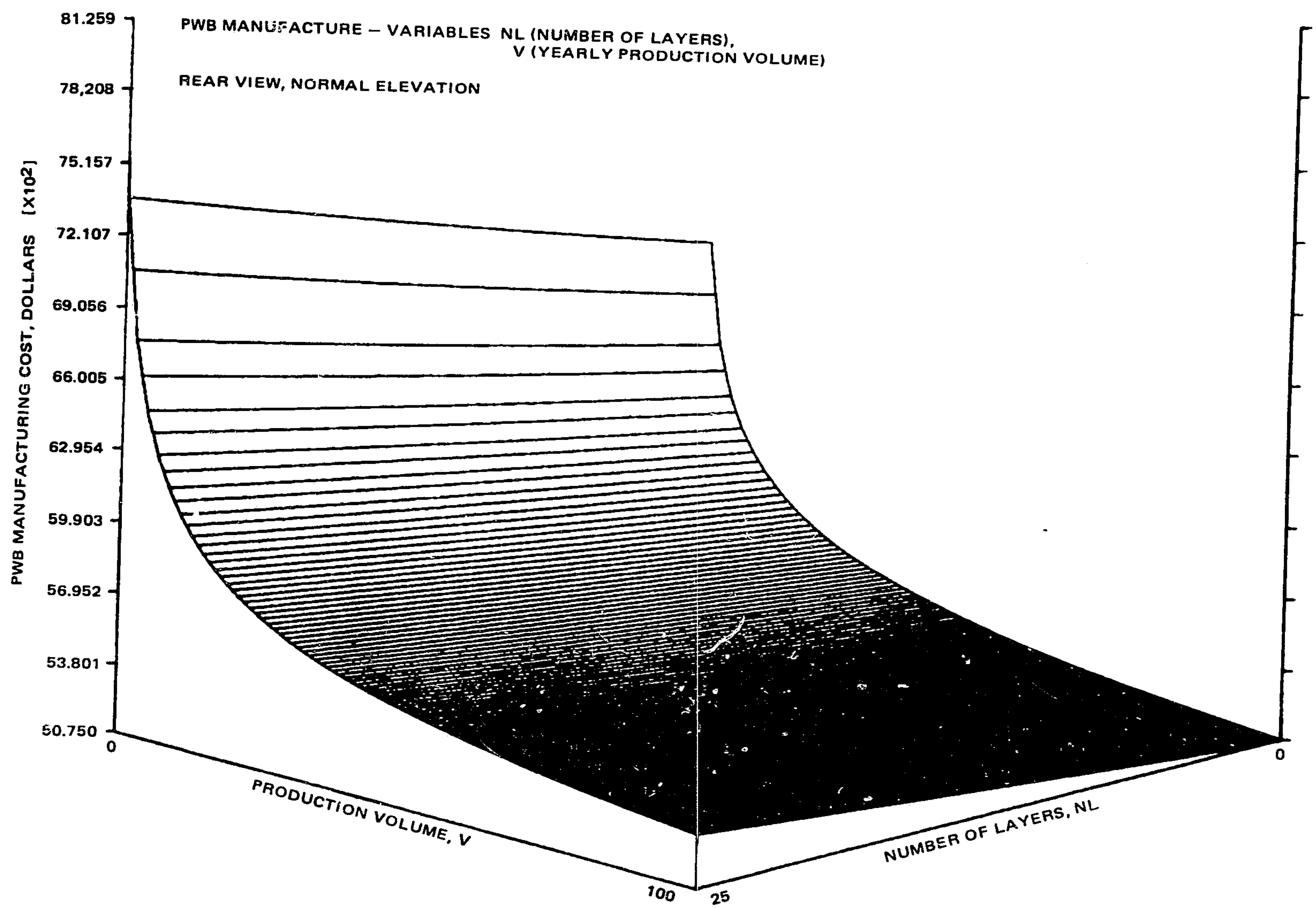


Figure 2-17. PWB manufacturing cost (fabrication and assembly) as a function of number of layers and production volume (rear view).

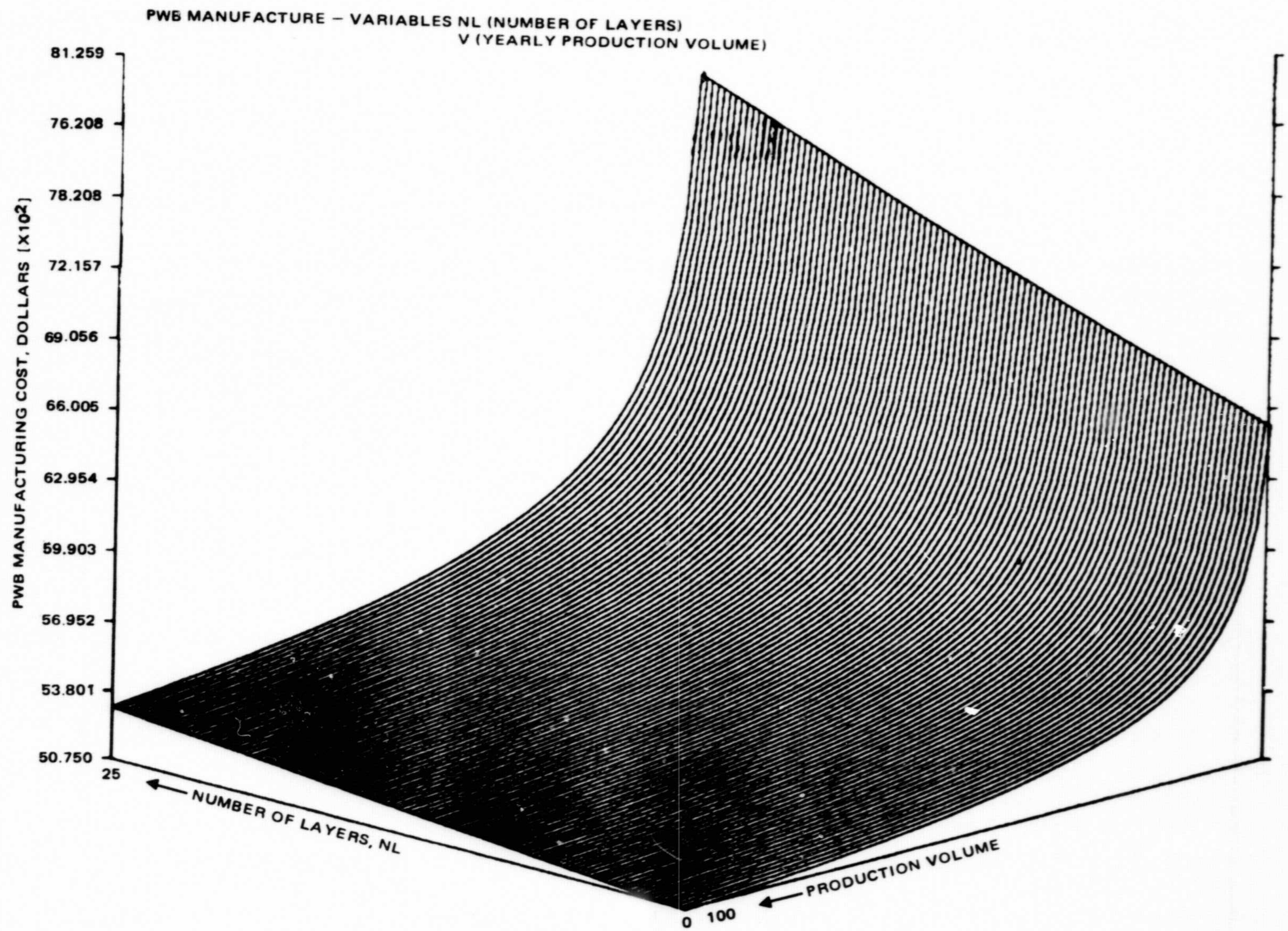


Figure 2-18. PWB manufacturing cost (fabrication and assembly) as a function of number of layers and production volume (left view).

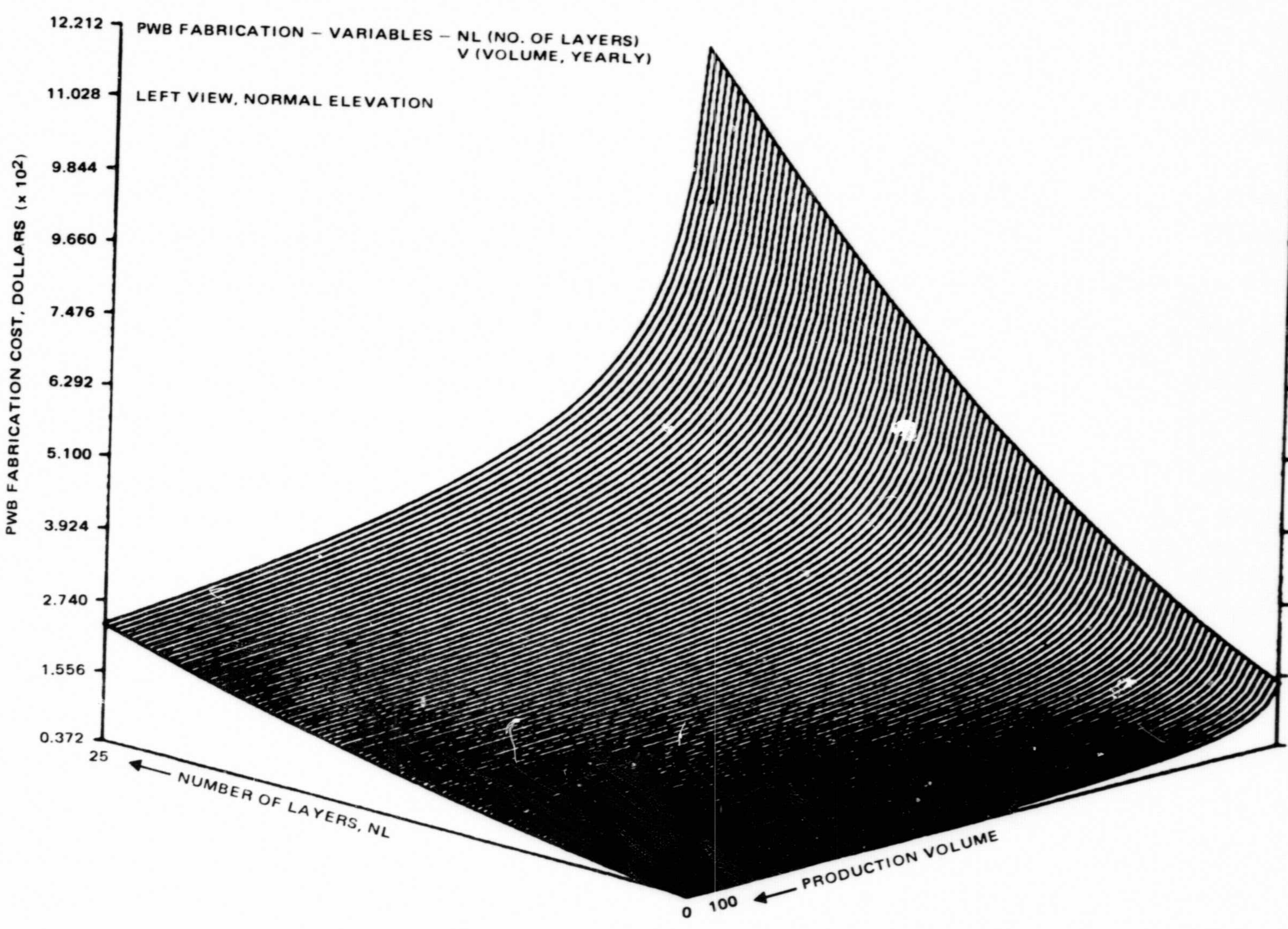


Figure 2-19. PWB fabrication is a function of number of layers and production volume (fabrication only) not including assembly.

implementation must be readily accessible. The three-dimensional display of cost functions, developed under this program, is one methodology for effectively transfering information from mathematical algorithms to the point of implementation.

The study of cost surfaces eventually will lead to a classification of cost factors and model types which are invariant for given sets of electronic systems (or technologies). Specific cases then can be deduced from these invariant sets of surfaces, and with the appropriate boundary conditions which identify a given electronics module, appropriate mathematical equations can be formulated.

It is proposed then to undertake a study of the properties attributable to cost surfaces. A question such as: "Could hybrid microelectronics packaging technology be combined with conventional PWB packaging to form an entirely new type of electronics packaging methodology? ", could be answered by taking representative surfaces for the two existing technologies and deforming them until they overlapped. If overlapping is obtained with a permissible deformation process, then the deformation parameters will be representative of those technological changes which make possible a unification of the two differing technologies. The development of cost surface analysis techniques will be extremely beneficial; especially in those fields of electronics where growth depends upon the convergence of several apparently-differing technologies.

2.2 TASK B - TAPE CHIP CARRIER (TCC) DEVELOPMENT

The emphasis over the past six months has been to continue refining existing processes, and to initiate new processes and equipment designs in order to improve yields, improve product reliability, and increase productivity. This expanded view of Task B and its goals resulted in faster, better, and more versatile methods for many of the tape and wafer fabrication steps.

The main approach has been to process at least three to ten tape strips at a time, of increased lengths ranging from 14 inches to three times that (or 42 inches), instead of the individual one-tape-at-a-time means. Still other approaches allow the initial processing of uncut tape carriers with special reel-to-reel stations. The usage of larger tanks provides the ability

to plate, develop, strip, and rinse more tape strips at a time, and in a manner which is more effective than that used before. Special film handling fixtures, ovens, hangers, cutters, splicers, and cleaning equipment now are either in use or being installed to better control and expedite the processes involved. Additionally, up-to-date digital-reading electronics equipment is being used, and wherever possible, standard 35-mm motion picture equipment is employed.

2.2.1 Tape Process Refinement

The general processing procedures for tape carriers basically remains the same, with changes made mainly with respect to the use of new, more effective equipment, and increased tape strip lengths. With reference to the block diagram of Figure 2-20, and beginning with the initial cleaning step, a reel-to-reel station (shown in Figure 2-21) is being used to run continuous uncut or other strip lengths as desired through special felt pads, saturated with a cleaning solution (Ammonium Persulfate); then onward through an atomized distilled water spray rinse (shown in Figure 22) or into a distilled water bath.

Tape Photolithography

The drying or photoresist prebaking of the tape can be done ten at a time, using any length up to 42 inches, within either the standard Blue M oven (shown in Figure 2-23A) or within the film drying oven (shown in Figure 2-23B), secured by means of a special hanger. These process improvements provide greater tape throughput with much less handling time, thereby permitting increased yields.

Roller-coating wet photoresist with the Gyrex Type 9 Microcoater remains the same as reported in the Interim Report[2], (Figure 2-13, page 2-27), except that a fixture has been added (shown in Figure 2-24) which accepts 14-inch tape strips in lots of 10 for baking-on the photoresist, and for transporting the strips between labs. With this fixture, less oven space is needed, and less handling is required; but moreover, there is no more damage due to sliding strips. To better achieve the 14-inch-strip capability, a special cutter has been constructed (shown in Figure 2-25) to accept reels

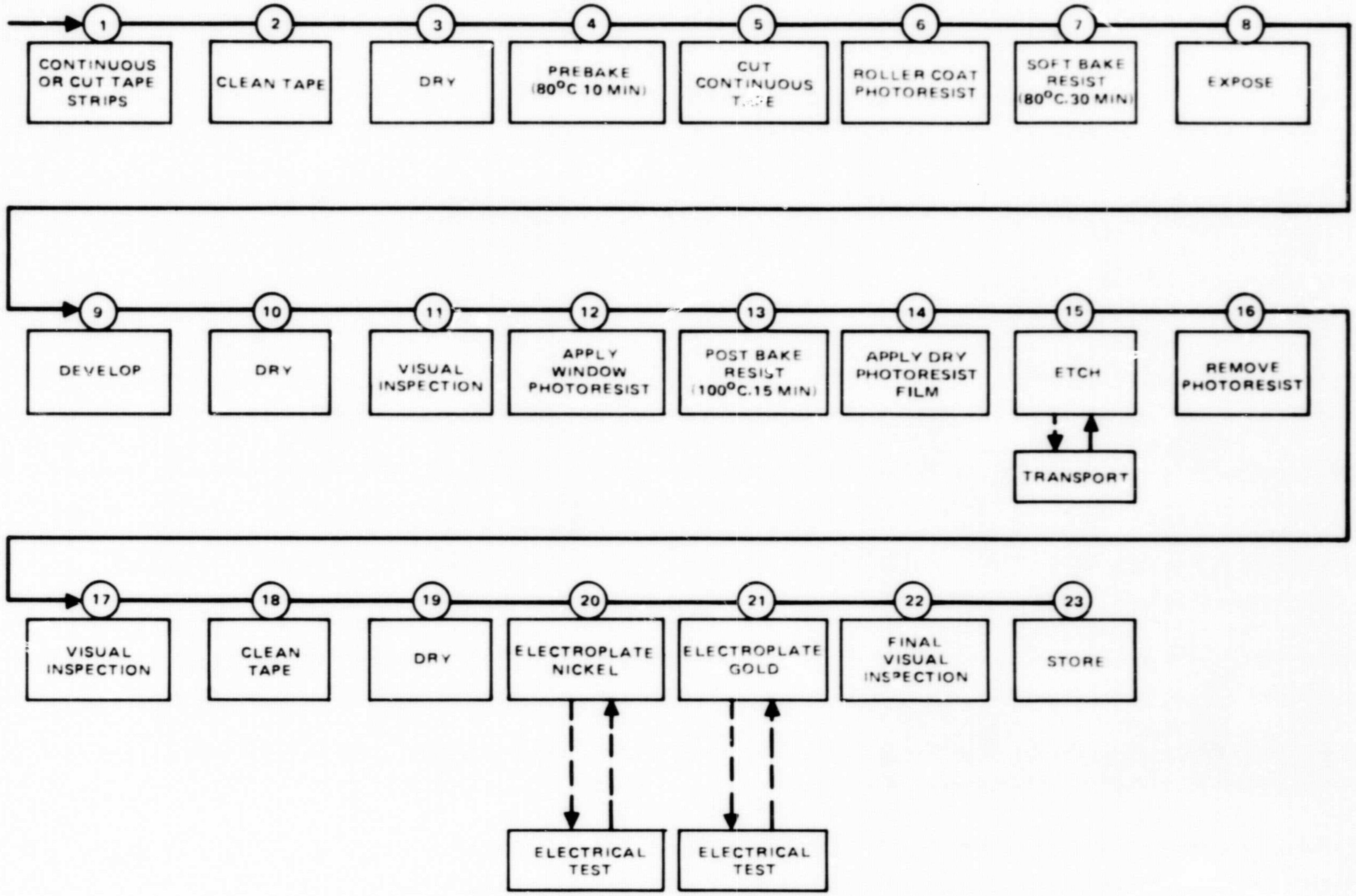


Figure 2-20. Updated tape carrier process flow chart.

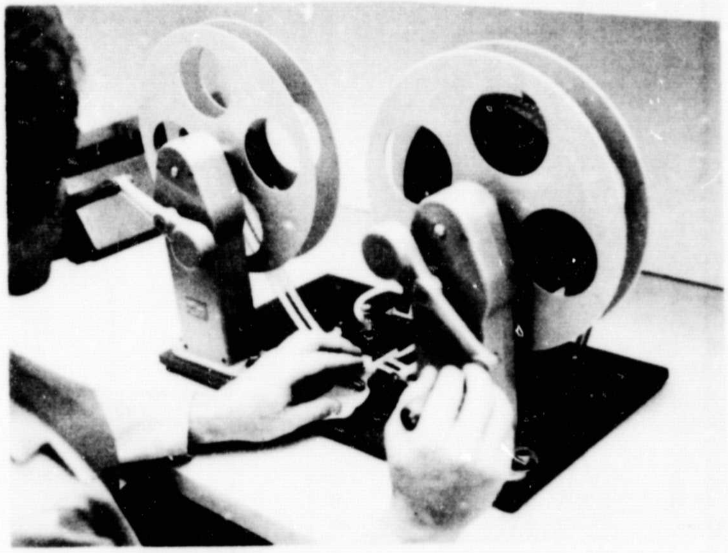


Figure 2-21. Tape chip carrier reel-to-reel pre-cleaning.

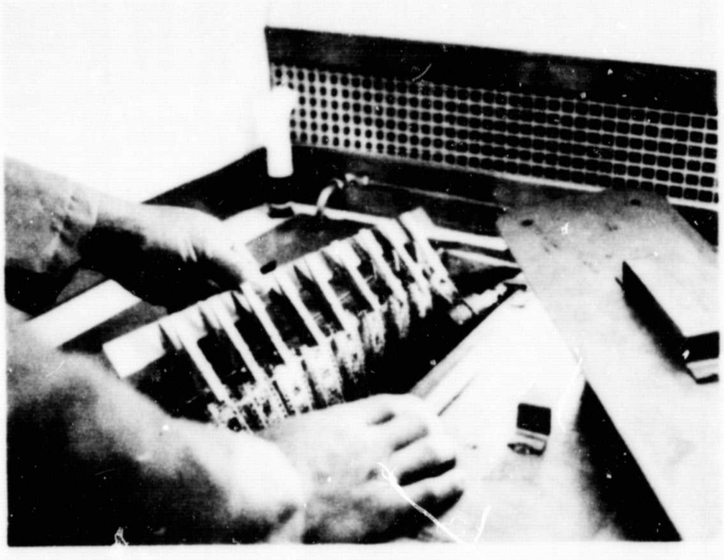
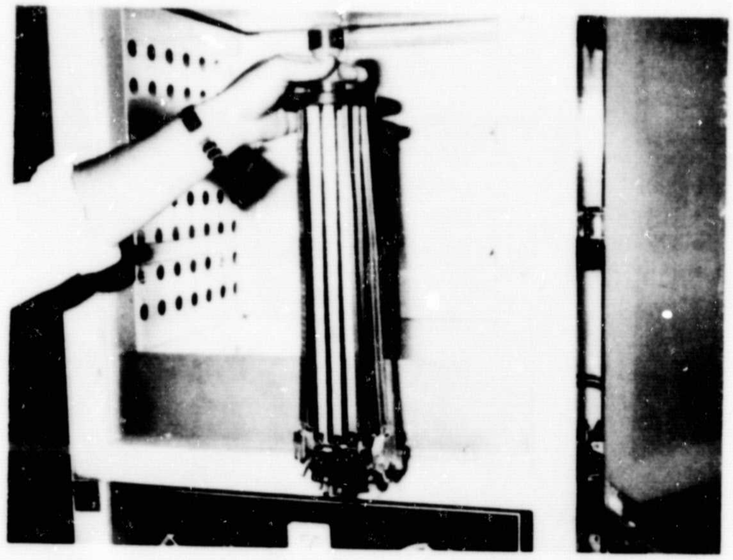


Figure 2-22. Atomized spray rinse station.



a. Ten tape carrier strips drying in Blue M oven

b. Ten tape carrier strips being processed in drying ovens

Figure 2-23. Improved tape carrier photoresist drying/pre-baking.

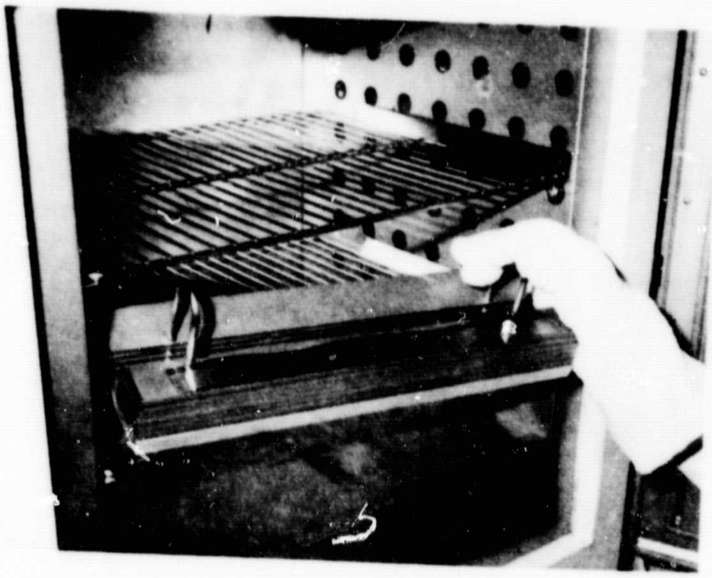


Figure 2-24. Wet-resist drying fixture.

Figure 2-25. Tape cutting fixture.

of tape as received from the vendor in lengths up to 1000 feet, to measure out the strip lengths desired, to repeatedly cut these strips square, and to hold the free end from the reel ready for the next cut. The cut strips are of equal lengths, and the entire cutting operation takes place in a much shorter time period, and with less handling.

Alternatively, a new concept of roller coating with 42-inch strips is being studied. The use of a transport tube (shown in Figure 2-26) will provide a means of holding 10 strips around a six-inch-diameter plastic opaque tube, utilizing another outer opaque cover for traveling between labs, for drying, and when etching. This tube concept will be reduced to practice during the potential follow-on program to be proposed as Supplementary Agreement No. 3.

The exposure station has been redesigned to accommodate a special vacuum frame (shown in Figure 2-27) which holds three of the 14-inch strips, and with more intense lamps replacing the previous 400-watt mercury vapor light source. Replacement of the mercury vapor lamp with a 4500-watt UV system has decreased the exposure time to less than half that required earlier (from 270 to 120 seconds). Usage of the new vacuum frame triples the throughput; but moreover, the three tape patterns etched into the frame provide the standard 35-mm sprockets and site supports to improve tape handling. This fixture also facilitates the use of 35-mm film photomasks, which are an attractive alternative to the usage of mylar sheet film photomasks, in that the former includes inherently-built-in alignment accuracy brought about by pre-punched sprocket holes. In addition, being of standard 35-mm film, they can be used for exposing tape by means of a closed-loop concept which permits hands-off, automatic program processing as shown in Figure 2-28. A digital LED displaying counter and opaque standard 35-mm leader tape are used here, together with photo-optical sensors (shown in Figure 2-29) to pick up the sprocket holes, to count between exposure frames, to count the number of sites exposed, and to shut off the system when the run is completed. This closed-loop concept is being investigated for implementation during the potential follow-on program to be proposed as Supplementary Agreement No. 3.

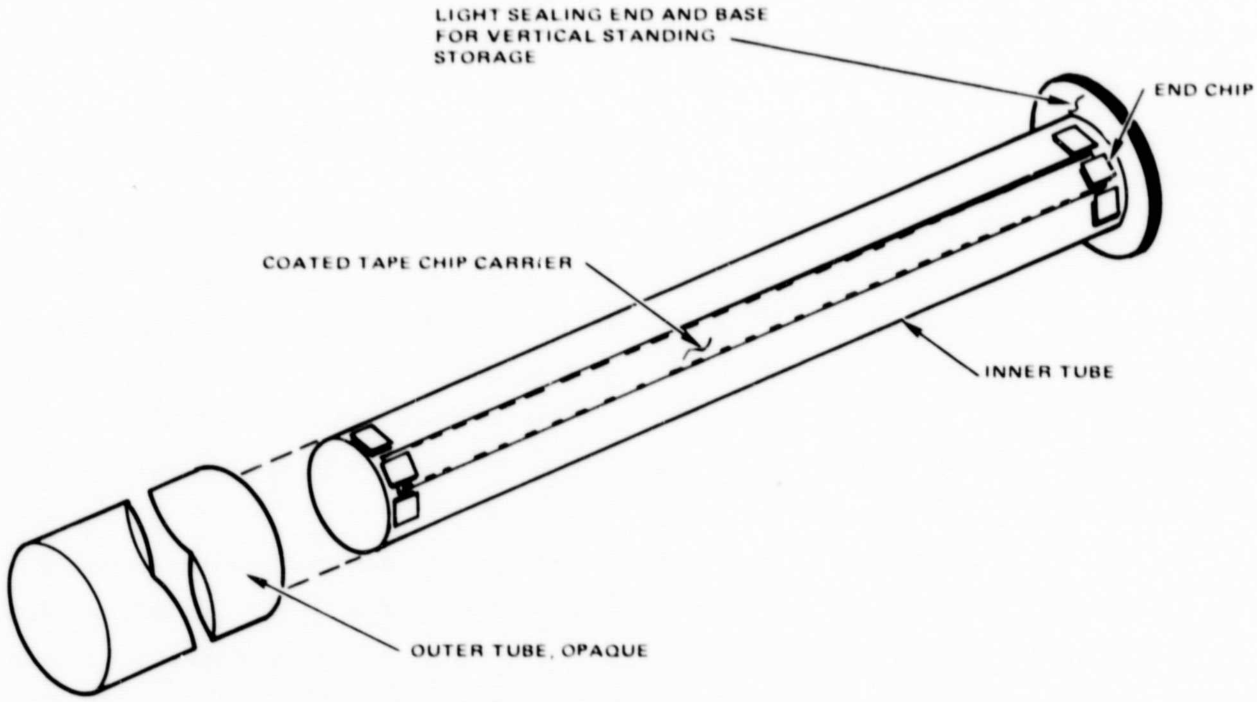


Figure 2-26. Proposed tape transport tube.

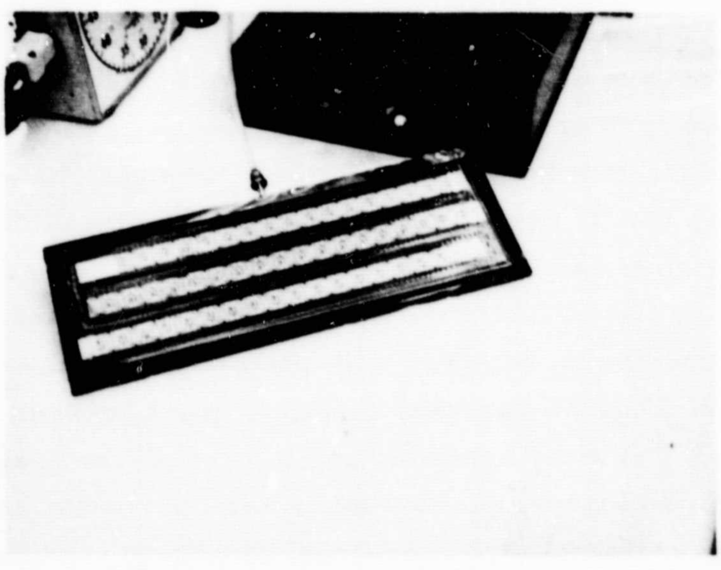


Figure 2-27. Three-strip vacuum-exposure frame.

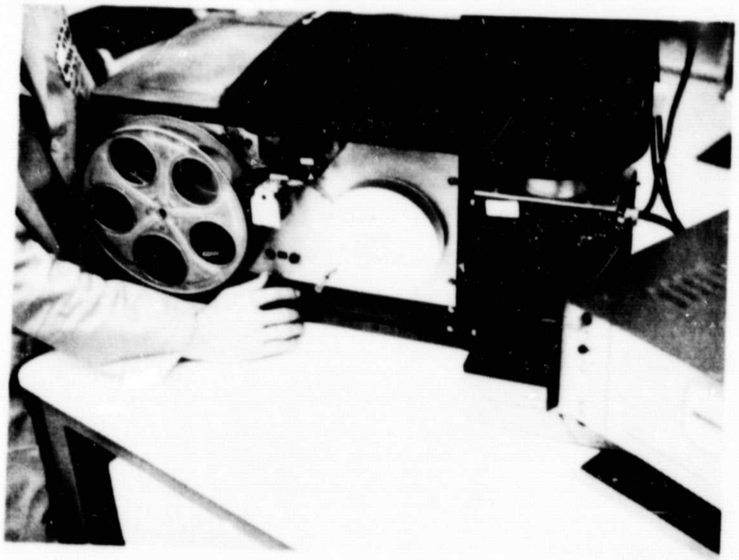


Figure 2-28. Concept of automatic closed-loop 35-mm photomask-and-tape-chip-carrier exposure system.

Figure 2-29. Closed-loop 25-mm digital display and photo-optical infrared sensor

Large stainless steel tanks with temperature controls and a dry nitrogen bubbler agitation system have been added for wet photoresist development, dry photoresist development, photoresist removal, and spray rinsing (shown in Figure 2-30). Each tank is capable of handling 10 or more 14-inch tape strips at one time to improve productivity. Moreover, usage of controlled heat and agitation permits more uniform and repeatable development times. The purpose of the agitation system in the photoresist remover solution is to accelerate the process; again improving productivity.

Application of Shipley Type AZ1350J photoresist to the polyimide window to compensate for the "tent" effect (Interim Report[2], paragraph 2.2.1, page 2-19) has been improved, both in its uniform coverage and its application speed. The liquid resist is applied by dispenser means to the five-mil stepped areas, rather then by hand brushing. A brush is used only for touch-up, and then with a single-stroke technique made possible by using window-size, 6-to-12-mm-wide brushes. Also, a new reel-to-reel tape handling station (shown in Figure 2-31), or a three-strip holding plate (shown in Figure 2-32) can be used. Both approaches reduce the handling time significantly, lessen damage, and thus again improve yield.

Photoresist postbaking has been reduced from 125°C to 100°C, and is followed immediately by the dry resist lamination. The new temperature was selected for its compatibility with the new window coating method, and to be compatible with the 100°C lamination temperature of the Riston Type 218R photoresist. By laminating immediately, the Riston conforms better to the geometric step of the window, giving better protection from the etchants in lead-defining later on. Although either 42-inch or 14-inch tape strips can be laminated, the shorter length has a wider alignment tolerance, and thus permits achievement of the best yield.

Tape Etching

Etching has remained unchanged with continued use of the Chemcut Model 547 Spray Etcher. Two designs are underway however, to improve productivity. The design of a tape strip holder for securing the longer 42-inch lengths eliminates many of the taping and cutting operations presently required. The proposed alternative design is to process reel-to-reel with the Western

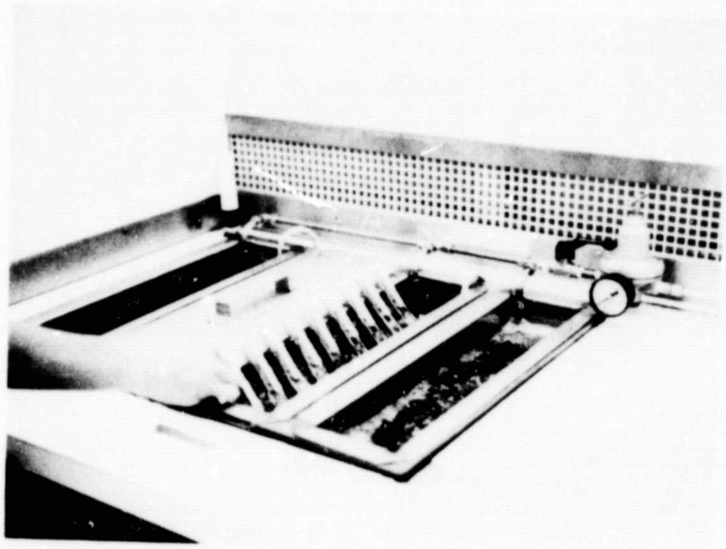


Figure 2-30. Wet photoresist developing, dry photoresist developing, and co-resist removal stations.

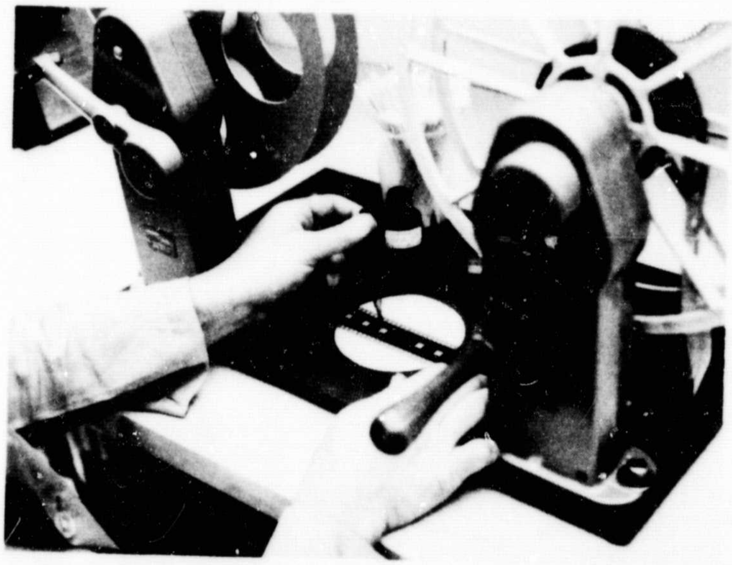


Figure 2-31. Resist dispensing on continuous tape chip carriers with reel-to-reel station.

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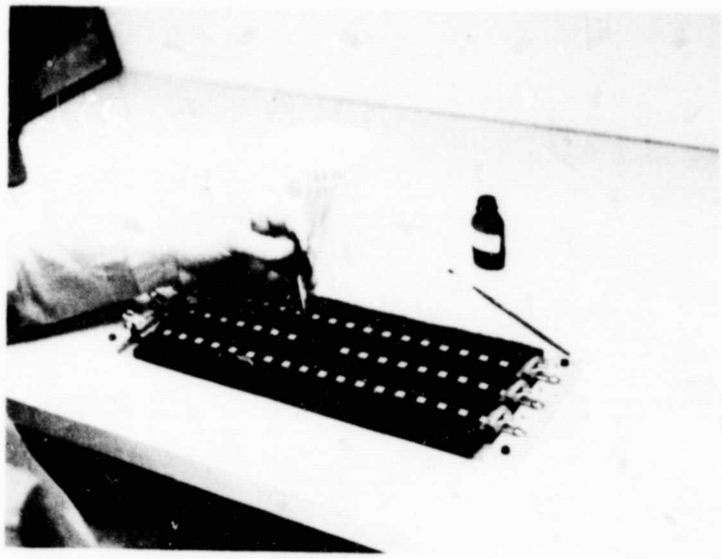

Figure 2-32. Photoresist dispensing on tape chip carrier strips.

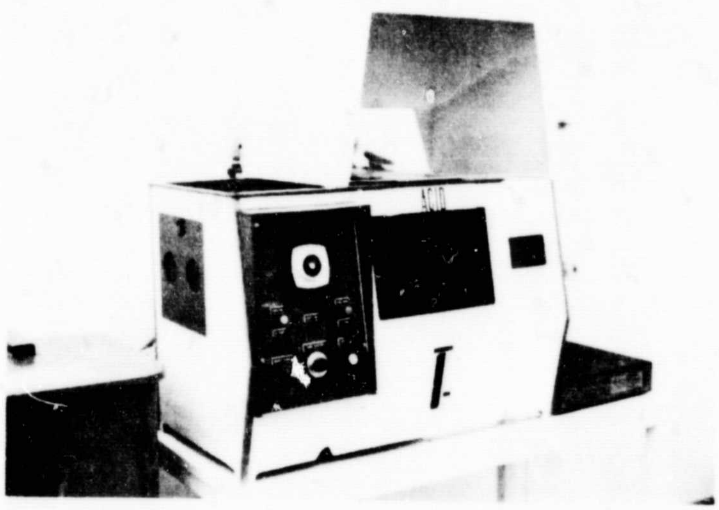

Figure 2-33. Western Technology Association Dynamil VRP50 spray etcher

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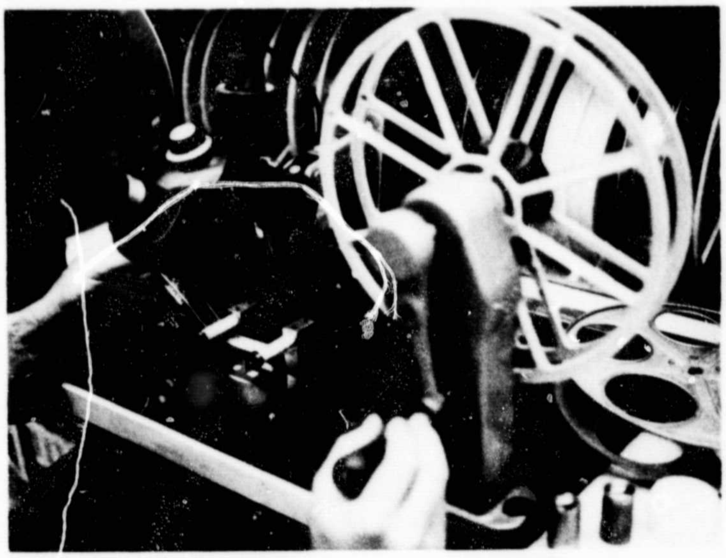
Technology Association Dynamil VRP 50 Spray Etcher (shown in Figure 2-33), using pneumatic or hydraulic atomized spray heads, with a motorized 35-mm motion picture rewind system. Usage of the atomized spray for the etching and follow-on DI-water rinsing steps will reduce liquid spray pressure on the leads, thus reducing damage and increasing yield. The atomized spray has been evaluated, and will be installed as a standard processing technique during the time period to be proposed as Supplementary Agreement No. 3.

Visual inspection can be accomplished with separate tape strips, or as a continuous spliced length on a new reel-to-reel inspection station with a built-in 7-to-30X zoom microscope; built-in illuminator with intensity selection; adaptor selection for other IMI reels, standard 35-mm 400-foot reels, or 35-mm 1000-foot split reels and with either square, round, or core-type centers (shown in Figures 2-34A and 2-34B). This station increases productivity, and because handling is reduced, it also increases yield.

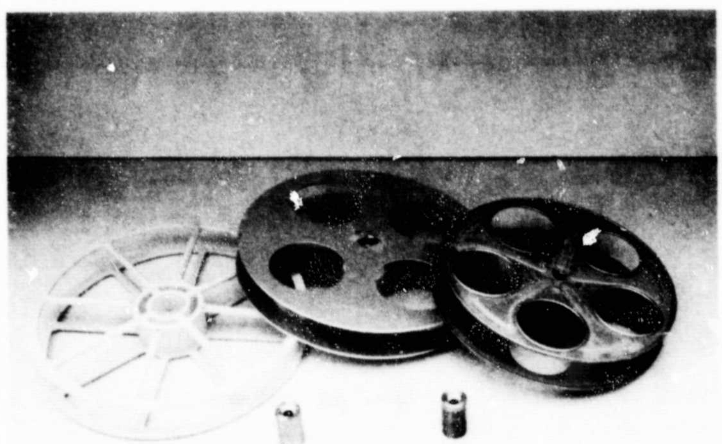
Tape Plating

A number of improvements have been made with respect to tape plating processes. These improvements result in better yield, and also in enhanced versatility. New gold and nickel plating tanks, complete with plating apparatus (shown in Figure 2-35), and an improved power control console shown in Figure 2-36) have been placed into operation for this purpose. Only the gold plating set-up currently is being utilized; both plating baths have been equipped to handle from six to ten 14-inch tape strips; to allow mixing of lead patterns; to provide capability for setting plating currents on an individual basis, and to utilize temperature-controlled quartz heaters in combination with recirculating pumps to provide more uniform plating coverage.

The concept of motorized tape-strip-holder agitation in each plating bath has been implemented to provide more uniform plating results, and the usage of liquid level sensors will prevent run losses caused by insufficient or unbalanced (evaporated) plating solutions. New Ph indication measurements now are used to assure better bath control, and all plating currents are indicated digitally and continuously to reduce meter reading errors. Separate ten-turn counting dial controls are provided, along with a ten-jack



a. Tape chip carrier visual inspection station for strips or continuous reel-to-reel usage



b. IMI reel, 35-mm 1000′ split reel, and 400′ standard 35-mm movie reel, with center adapters for reel interchangeability

Figure 2-34. TCC reel usage.

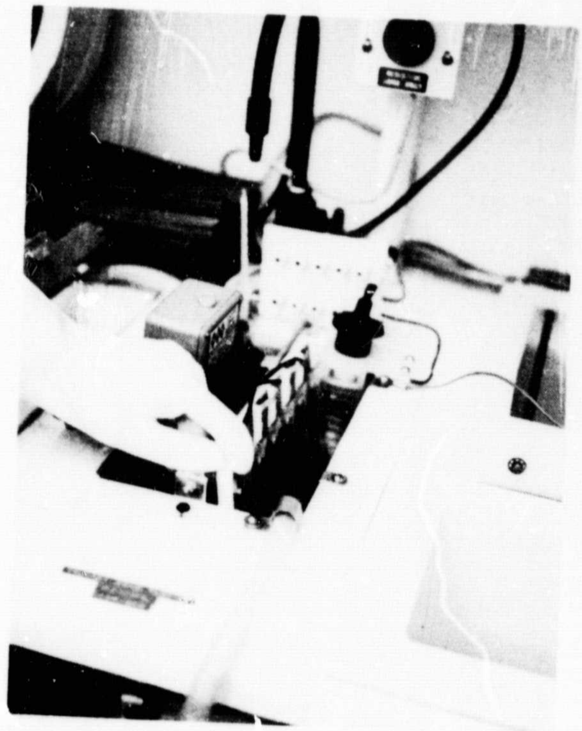


Figure 2-35. Improved plating tank set-up.

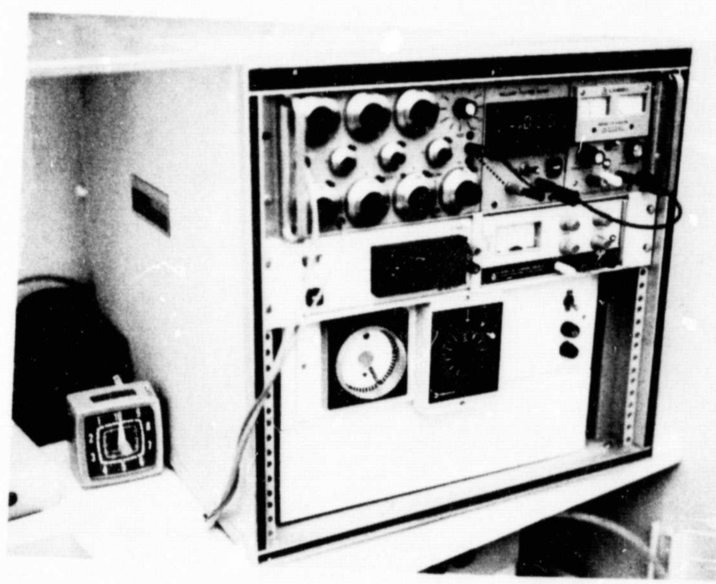
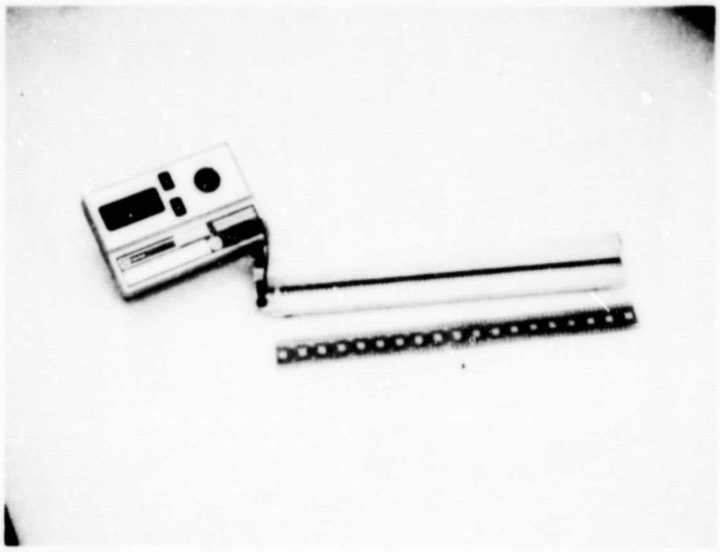
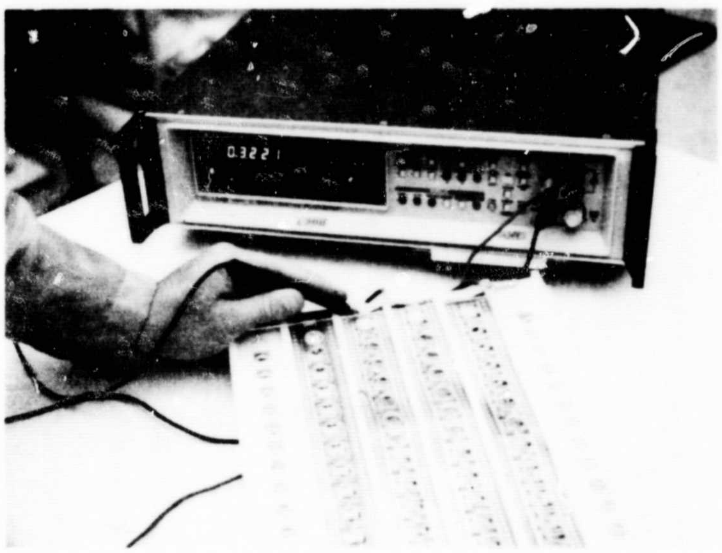


Figure 2-36. Plating control/power supply console.



a. Capacitance testing of etched tape strips



b. Measuring contact resistance of mounted tape strips with a Fluke Type 8502A resistance bridge

Figure 2-37. Plating set-up/monitoring equipment.

control panel for individualized selection and control of specific tape types. A capacitance test fixture (shown in Figure 2-37A) is being utilized to sense the etched pattern area so that initial plating current requirements may be determined more accurately. A Fluke Type 8502A Digital Multimeter (shown in Figure 2-37B) is being used to monitor reductions in current which are required for accurate plating control. Along with these measuring devices, three instruments are being used to check plated thicknesses so that specific plating time requirements may be determined. These include the Zeiss Light Section Microscope (shown in Figure 2-38), the Sloan Dektak (shown in Figure 2-39), and the Type DD-700 Betascope (shown in Fig Figure 2-40).

In an effort to further increase yield, the basic Honeywell-designed plating rack (shown in the Interim Report[2], Figure 2-14, page 2-27) currently is being redesigned, as indicated in Figure 2-41, to provide four additional plating positions (so as to be compatible with the ten-strip processing methodologies), to provide better individual contact capability, to be compatible with the ten-jack control panel circuitry, and to provide a hingeable Velcro-strip latching cover for quicker and less damaging loading and unloading operations.

Hughes tape chip carriers currently are being produced satisfactorily with only gold plating over the etched copper. The addition of a one-micron-thick plated nickel layer between the copper and the gold is being investigated however, for the purpose of preventing possible inter-diffusion of the gold and the copper, thus assuring lead integrity under potentially-adverse environmental conditions. A continuing investigation involving pull-strength testing of chips gang-bonded to tape chip carriers and to hermetic chip carriers will serve to determine whether addition of the nickel barrier layer will provide the best reliability and yield.

The reel-to-reel station is utilized again for final visual inspection. Designs currently are being made however, to co-reel etched and plated tape onto the standard IMI reel (shown in Figure 2-42), along with 35-mm standard movie leader utilized as a separator. A splicing station (shown in Figure 2-43) is utilized to connect all completed and acceptable strips into a continuous strip. Much time is saved and potentially-damaging handling is

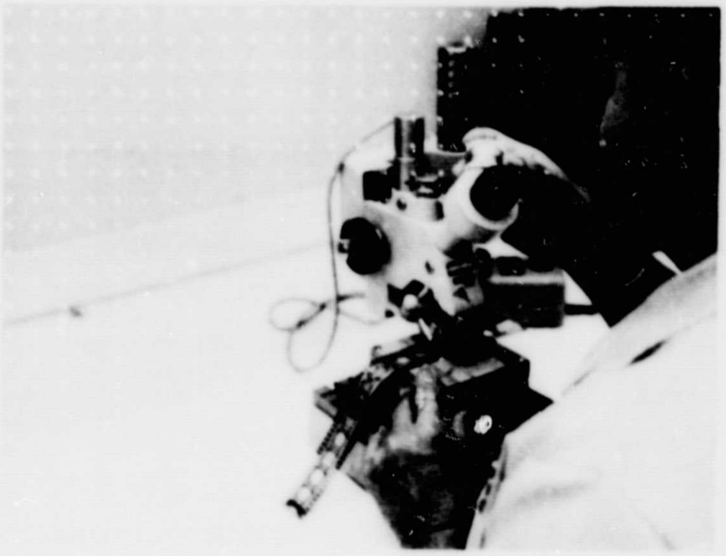


Figure 2-38. Plating thickness measurement with a Zeiss light section microscope.

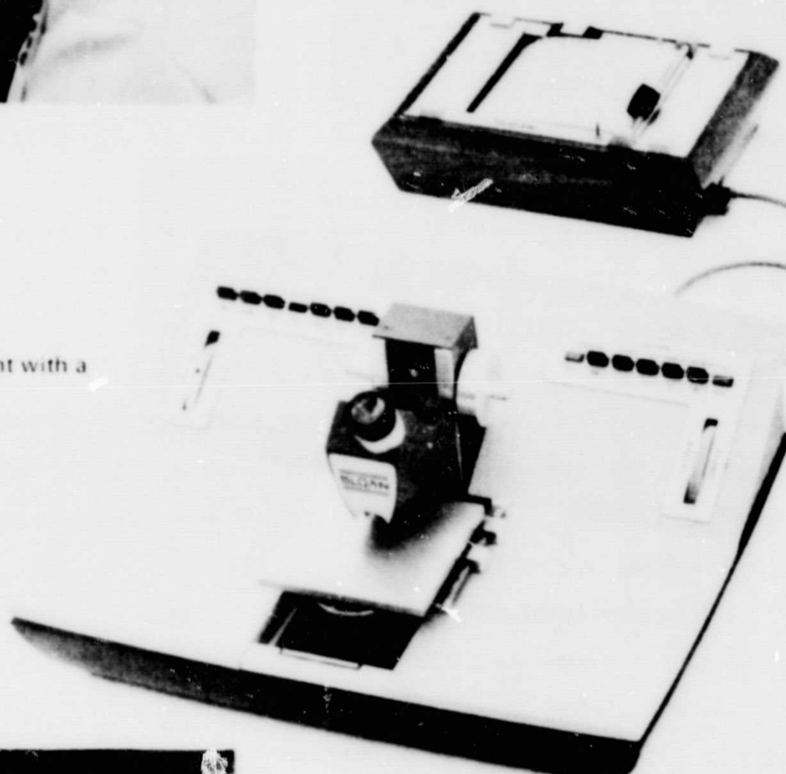


Figure 2-39. Plating thickness measurement with a Sloan "Dek-Tak" instrument.

Figure 2-40. Plating thickness measurement with a Model DD-700 Betascope.

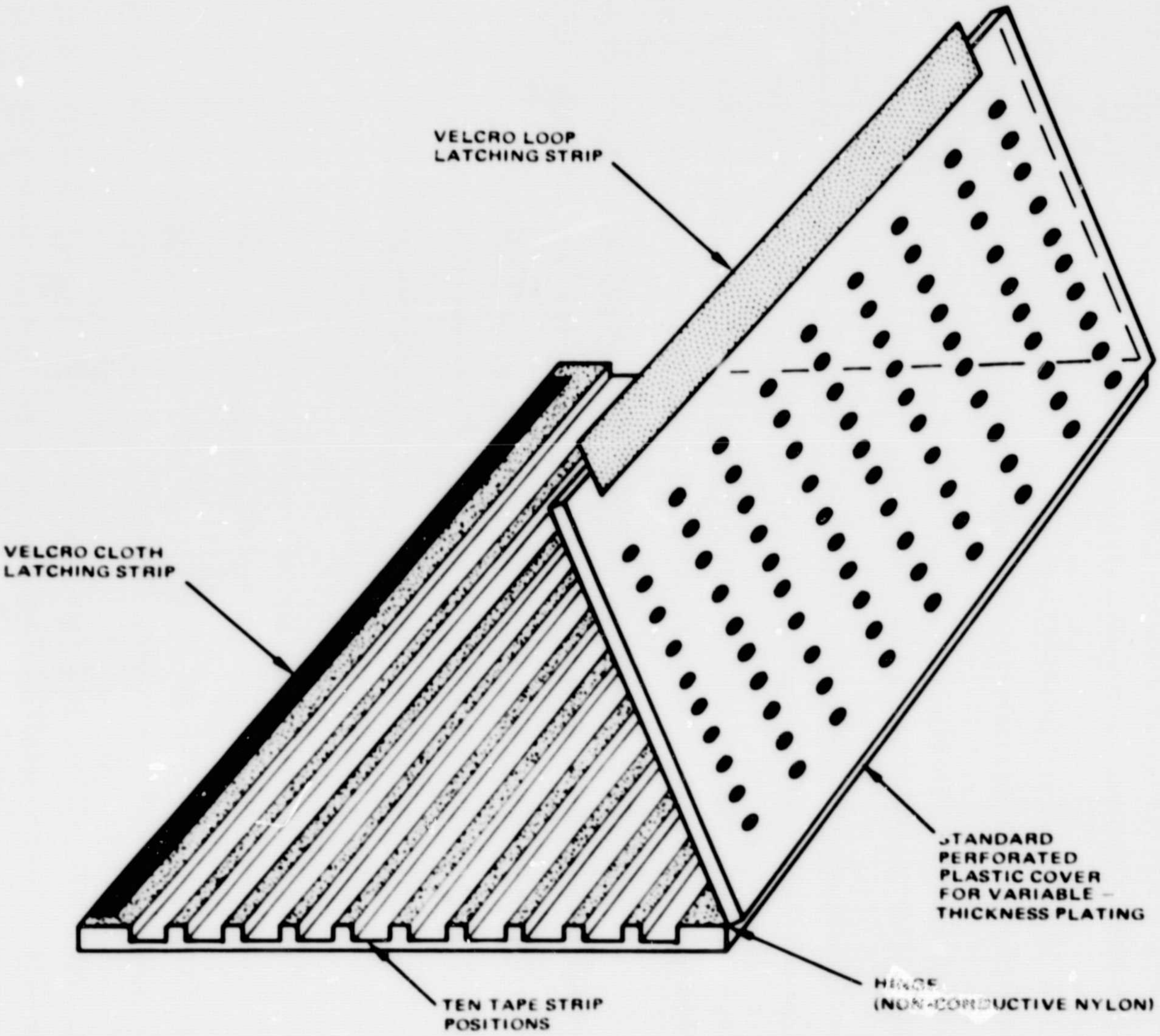


Figure 2-41. Improved plating rack design

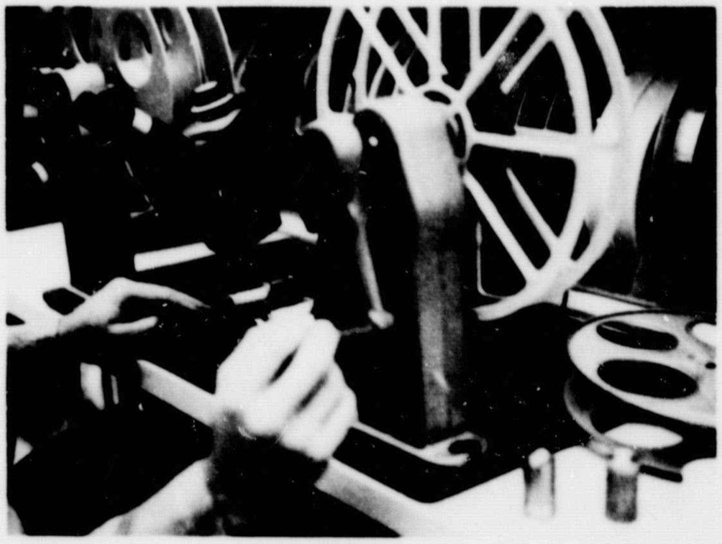


Figure 2-42. Co-reeling completed etched and plated tape chip carriers with 35-mm separator film.

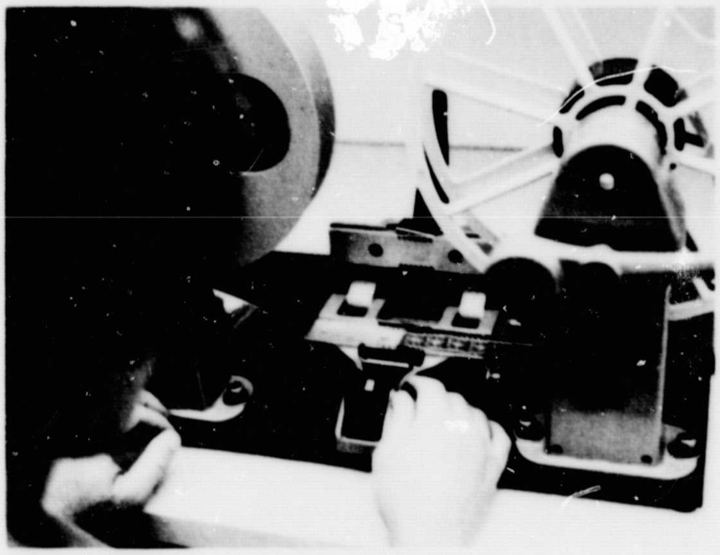


Figure 2-43. Splicing of completed tape strips with 35-mm leader film.

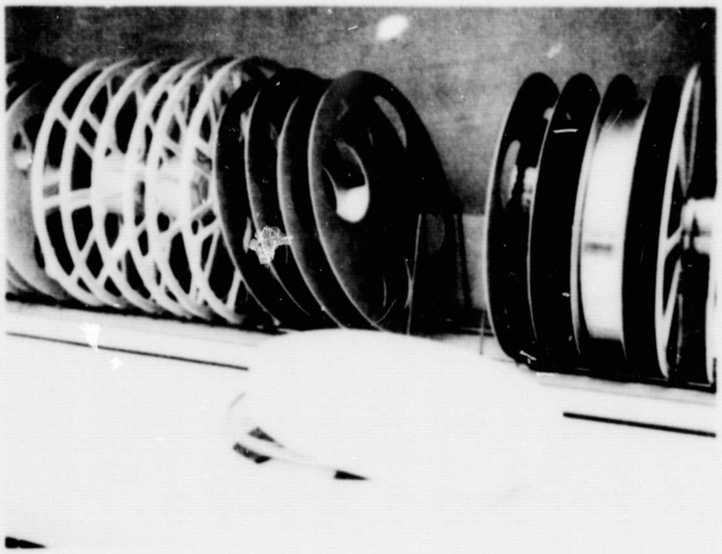


Figure 2-44. Tape, leader/separator film, and finished TCC storage.

reduced as a result of utilizing co-reeling and splicing techniques; the tapes are:

1. Now easily and safely stored within standard film cans (shown in Figure 2-44),
2. Take up minimum storage space, and
3. Are immediately available for use on the IMI Model 207 Inner-Lead Bonder.

Wafer Bump Process Refinement

Fabrication of a fountain-type plater (discussed in the Interim Report[2], Paragraph 2.2.2, pages 2-28/2-29) is progressing well. The major initial in-house design work has been completed, and assembly is in progress, as shown in Figure 2-45. The plater comprises three fountain stations, all fed from a non-filtered pump through three individual flow meters. Two cups or fountains accept either three-inch or four-inch-diameter silicon wafers; the third cup is intended for any wafer three inches or less in size. Usable remnants which may be broken from expensive large wafer patterns (or which may be shipped in mixed form by semiconductor suppliers desiring to suppress their yield information), thus can be utilized effectively. Usage of smaller wafer sections is made possible by multiple wiring of parallel-connected individually-spring-loaded contacts, as shown in Figure 2-46. Other special features to improve bump uniformity, to minimize height variation, and to promote good bump shaping, include the following:

1. An entrance chamber to create a more even and regulated pressure source,
2. A finely-perforated baffle to partially regulate the pressure; and to provide a uniform vertical flow rate across the inner tube area, upward through the anode screen, and onto the wafer, and
3. Large peripheral exit holes to assure more-uniform flow rate across the full wafer surfaces.

These improvement are shown in the diagram of Figure 2-46.

Outer anode contacts provide electrical connection without introducing contaminating contact materials which could affect the hardness (and thus the bond-ability) of the plated bumps. A secondary pumping system includes in-line filters to recirculate the plating solution continuously, and to remove

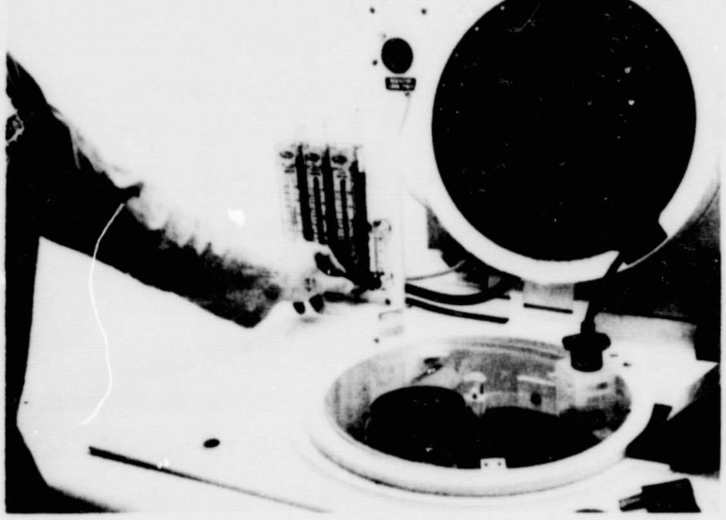


Figure 2-45. Wafer fountain plating station.

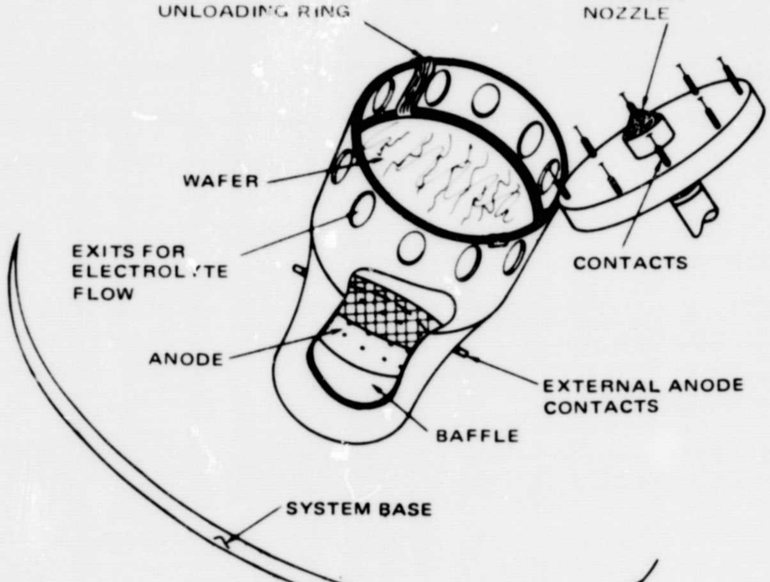


Figure 2-46. Fountain plater cup with spring contacts and peripheral exits for electrolyte flow

loose particles. This system (shown in Figure 2-47) pumps the solution around the outside of the three cups and around a quartz heater. This outer-bath circulation permits usage of a single heater for all the fountains. In addition, the outer bath acts as a buffer to the natural atmosphere temperature changes, and to the temperature changes of the cycling heater. As an added safety feature, this outer bath is used to sense and thermostatically control the temperature, and also to provide a level below which the system automatically will shut off. The result will be fewer unplated or thinly-plated bumps, currently caused by particulate contamination.

Currently, studies are continuing in an effort to improve adherence of the dry-resist pattern-plating film. There have been some lifting problems, contributing to partial loss of otherwise good chips. It is felt that a $100^{\circ}C$ preheating technique should be used on the wafer in a manner similar to that utilized for tape carrier strips (Figure 2-20, step 13). In addition, other cleaning and drying methods may be used. The need for these latter improvements is based on results of research studies of thin film deposition precleaning techniques. Toward this end, a cascade rinse station, shown in Figure 2-48, currently is being added.

2.2.2 ILB Process Refinement

During the time period covered by Supplementary Agreement No. 2, Hughes received a Model-207 production-grade Inner-Lead Bonder, purchased from International Micro Industries (IMI), Cherry Hill, New Jersey as a capital equipment item. This equipment, shown in Figure 2-49A, was selected over the more-widely-used Jade Corporation inner-lead bonder after a thorough competitive evaluation involving relative versatility, flexibility, adaptability to hybrid microcircuit applications, operational reliability, and overall effectiveness. The close-up view of Figure 2-49B shows a bumped wafer in place, with the matching tape carrier strip superimposed in the film carriage.

Checkout activities related to this machine were initiated during the first six-month period of this follow-on program, and have been continued at a relatively low level during the latter six-month period. Current Hughes tape chip carrier applications require only small quantities of inner-lead-bonded semiconductor devices. This minimized initial need to date has tended

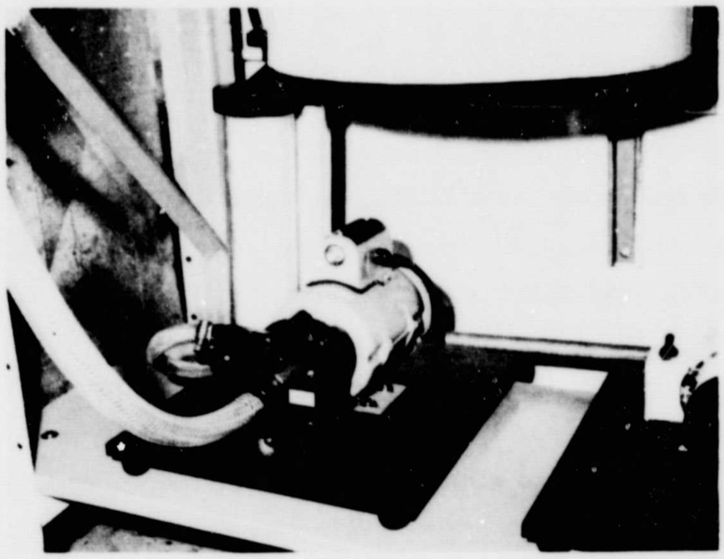


Figure 2-47. Fountain plater recirculation and filtering system.

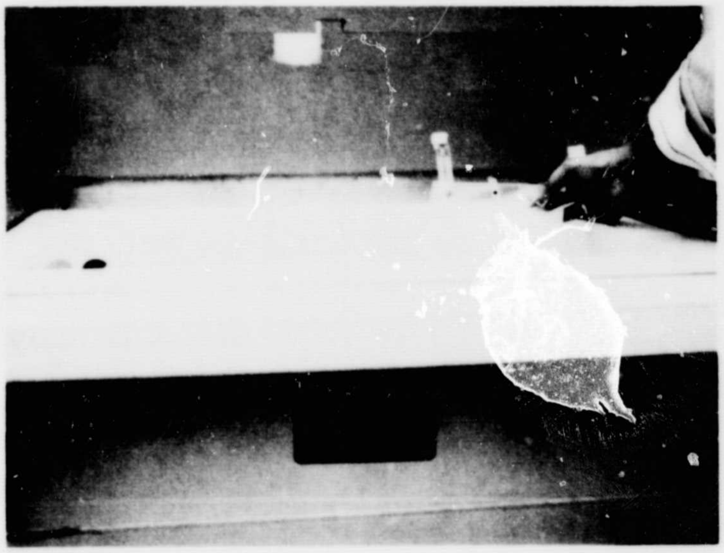
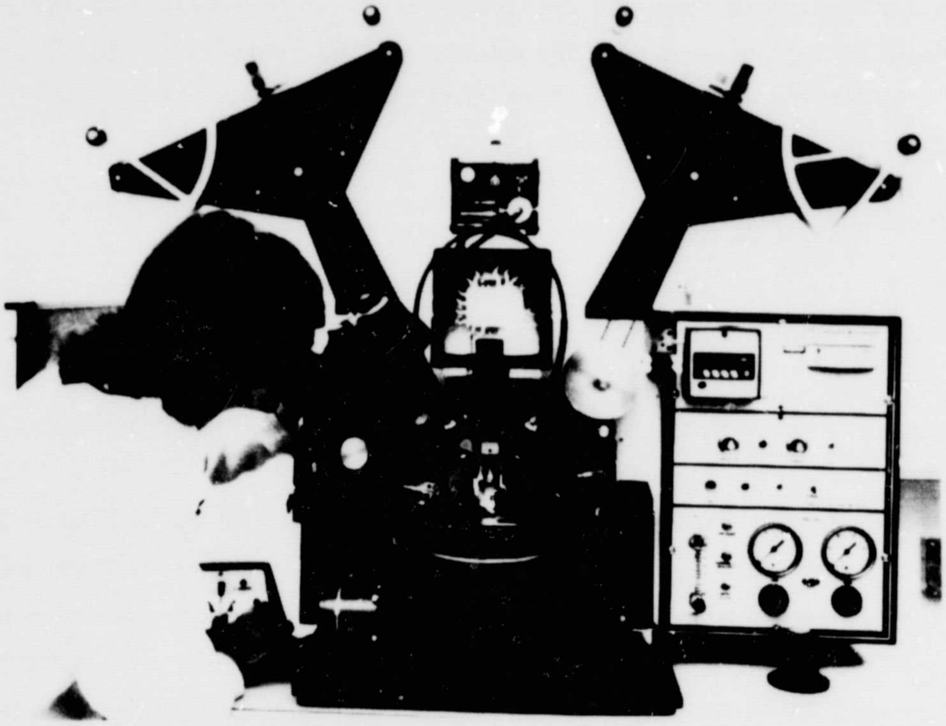
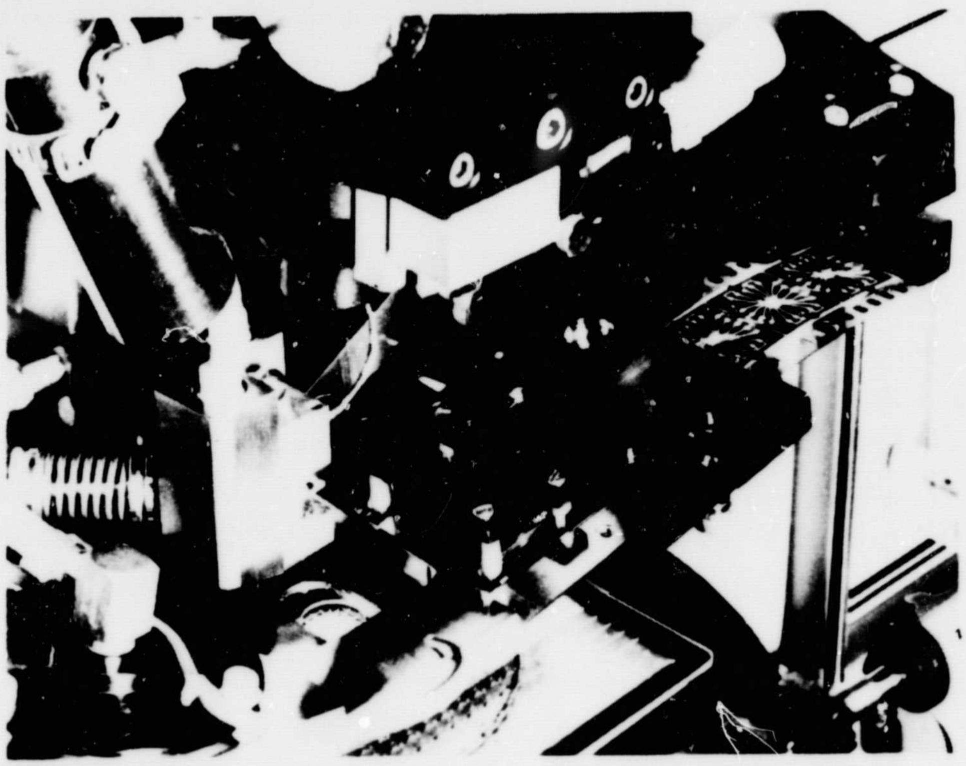


Figure 2-48. Cascade method of wafer rinsing.



a) OVERALL VIEW



b) CLOSE-UP OPERATING VIEW

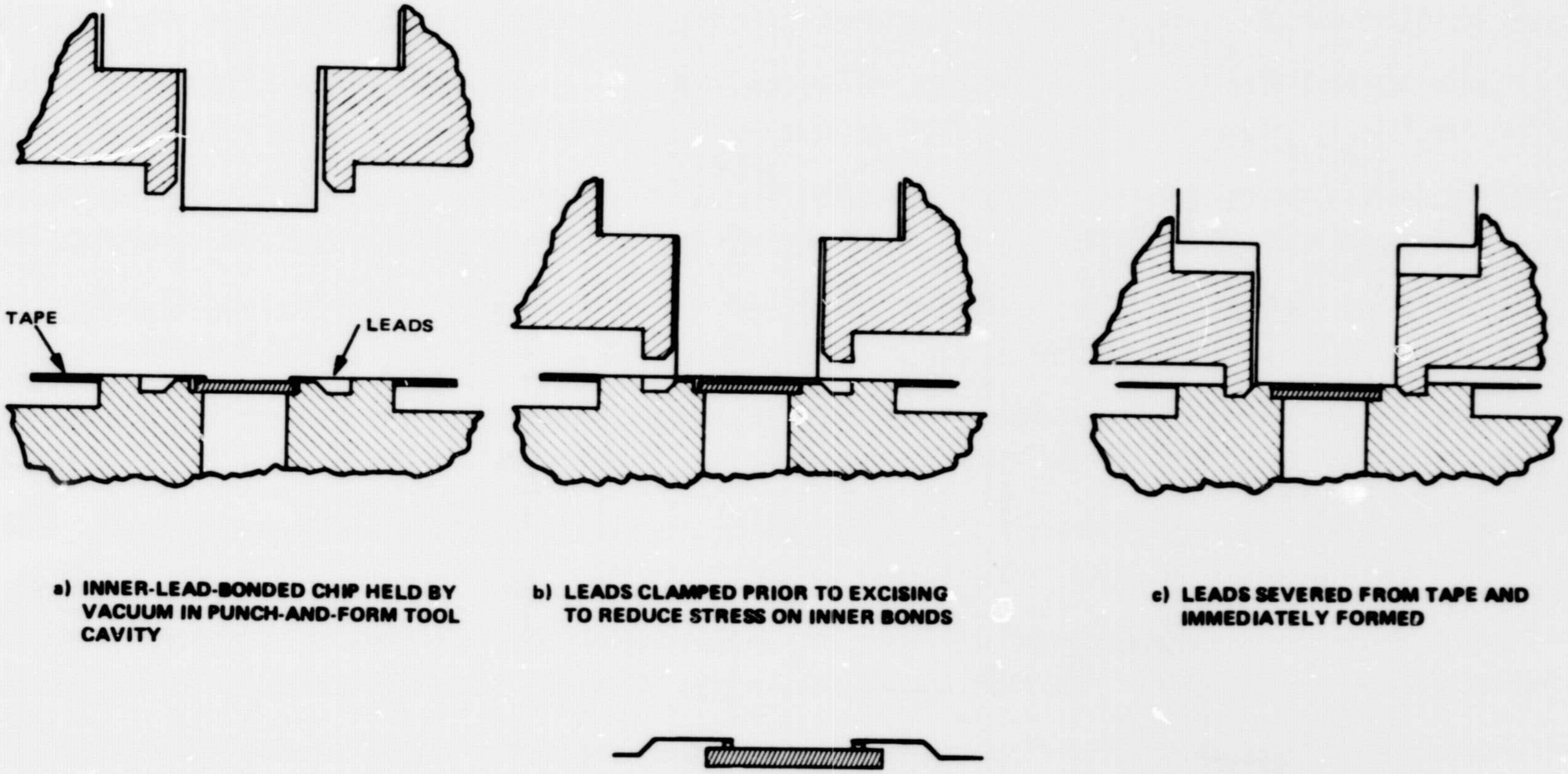
Figure 2-49. IMI Model-207 inner-lead bonder.

to discourage strong investment of relatively limited manpower toward detailed checkout of equipment which already has been proven effective in small quantity applications. As Hughes internal needs increase, ILB process refinement will be expanded.

2.2.3 OLB Process Refinement

During the time period covered by Supplementary Agreement No. 2, the combination excise/forming tool diagrammed in Figure 2-50 was designed and ordered through the Hughes Industrial Product Division (IPD), Carlsbad, California. An assembly drawing of this tool (which was delivered during August, 1979) is shown in Figure 2-51.

Hughes has procured a manual Outer-Lead Bonder from IPD. This bonder, shown in Figure 2-52, may be used in either a pulse-reflow-solder or a thermocompression-bonding mode. It utilizes a Hughes thermocouple-controlled AC power supply and a Hughes welding head fitted with a tungsten-carbide square-ring bonding tool. The unit is designed to supply a controlled "Time-At-Temperature" heating pulse, with separate time, temperature, and force adjustments. Its operation, shown in the close-up of photograph of Figure 2-53, involves vacuum pick-up of the "spider" (excised chip with formed tape-carrier leads attached); placement of the substrate (in this case represented by the hermetic chip carrier) through light-beam alignment; and outer-lead bonding by foot-pedal action: as the foot pedal is depressed, the vacuum quill and surrounding collet is lowered until the "spider" die makes contact with the substrate, on which an appropriately-located "dot" of epoxy has been placed. As the pedal is depressed further, the collet makes contact around the OLB lead periphery, and sufficient pressure is applied to activate the digitally-timed power supply, either in a pulse-reflow-solder or thermo-compression bonding mode. After pre-set heat and pressure is applied to make the bond, the preprogrammed power supply turns off, and cooling action takes place. At this time, the pedal is released, and the next "spider" assembly may be aligned for vacuum pick-up. A typical outer-lead-bond to a thin film gold metallization pattern requires a tool temperature of 450^{o}C, pulsed for one second at 17,000 psi per bump. Stage heating need not be used in this outer-lead bonding process.



a) INNER-LEAD-BONDED CHIP HELD BY VACUUM IN PUNCH-AND-FORM TOOL CAVITY

b) LEADS CLAMPED PRIOR TO EXCISING TO REDUCE STRESS ON INNER BONDS

c) LEADS SEVERED FROM TAPE AND IMMEDIATELY FORMED

d) EXCISED CHIP AFTER REMOVAL FROM PUNCH-AND-FORM TOOL

Figure 2-50. Combination excise/forming tool operation diagram

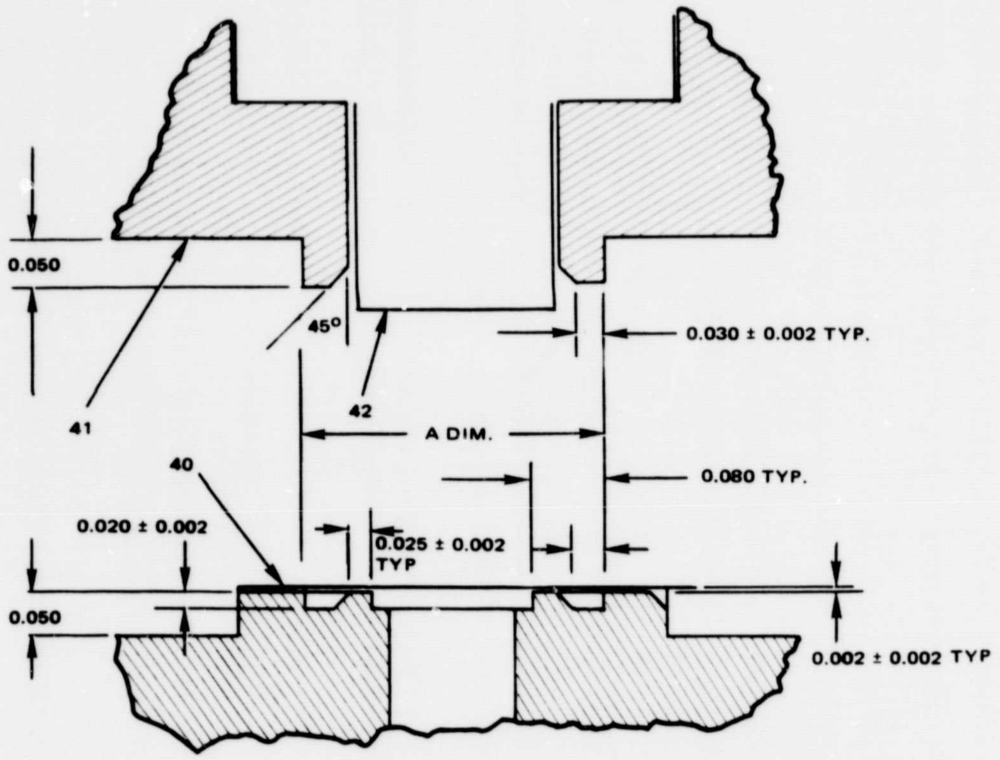


Figure 2-51. Combination excise/forming tool-assembly drawing

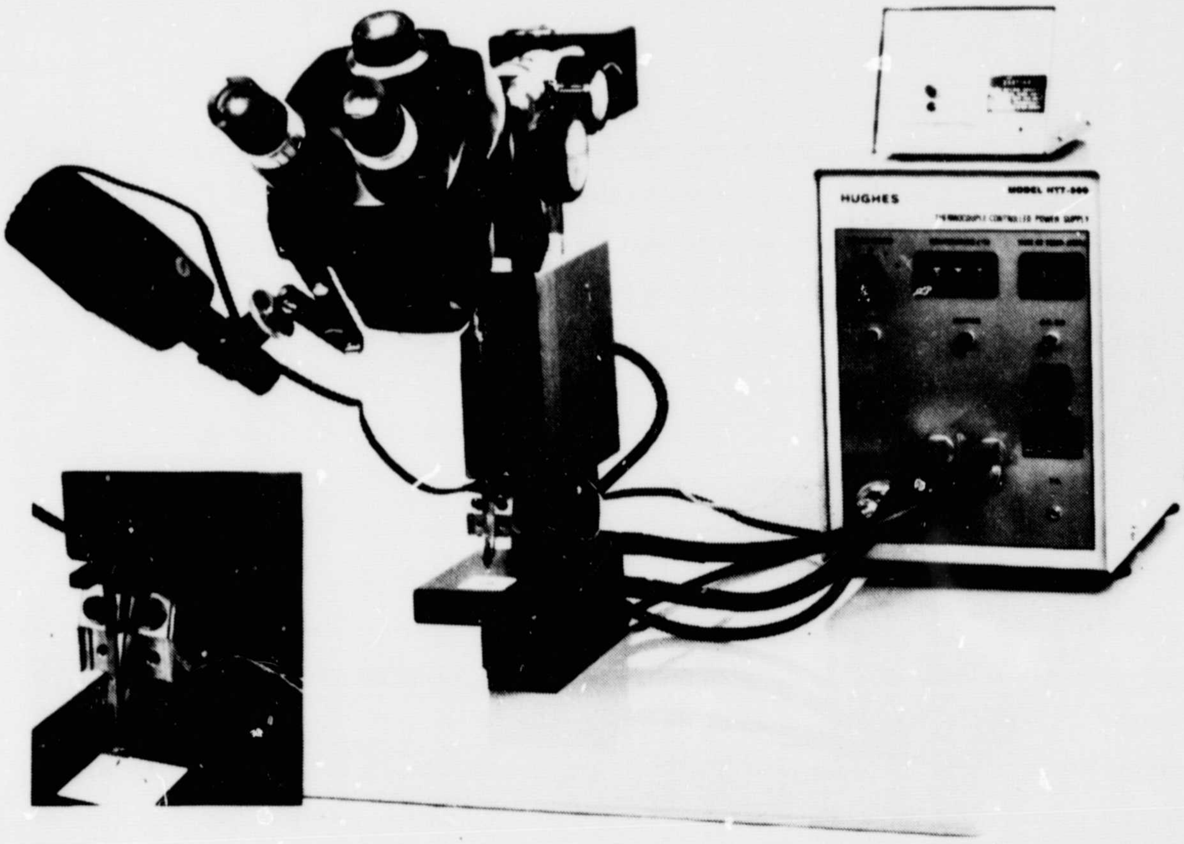


Figure 2-52. Hughes-IPD manual outer-lead bonder.

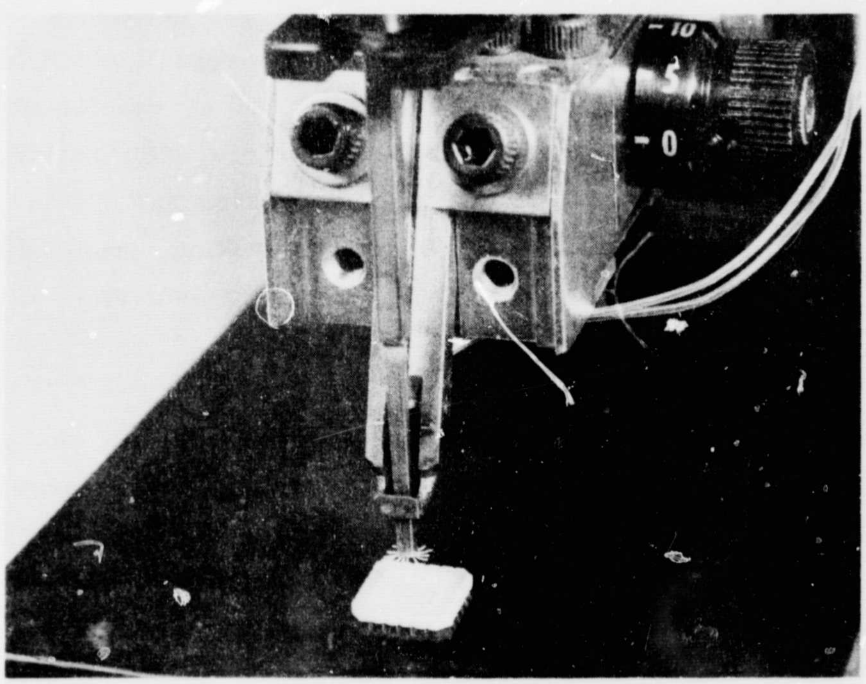


Figure 2-53. Close-up operation of Hughes-IPD manual outer-lead bonder.

This OLB concept readily will be adaptable to semi-automatic operation when capital funding becomes available. Hughes OLB activities currently are confined to those which can be accomplished with the manual unit. Appropriate tools have been ordered to demonstrate OLB processing of the semiconductor devices listed as A, B, C, and D in Table 1-1. The remaining OLB tools (including those required to demonstrate TCC processing of STAR devices) will be procured as the need arises for their use.

2.2.3.1 Pull-Test Results with Chips Mounted in Hermetic Chip Carriers

During the first six-month effort under Supplementary Agreement No. 2, Hughes Type HCMP 1824 wafers (32 x 8 Static RAMS) were bumped, inner-lead-bonded, excised, and outer-lead-bonded to standard 24-lead commercial-style hermetic chip carriers to form pull test samples. The bumped wafers exhibited a 75-to-90-gram bump shear strength, with all failures occurring as chip-outs in the silicon beneath each bump.

The size of the chip is 0.117 in. x 0.156 in., leaving a lead span of 70 to 105 mils within the chip carrier. Lead widths at inner ends varied from 4.0 to 4.5 mils. Double-bond pull testing was performed at a rate of four grams-per-second, with the hook gripping in the center of the span. The mean pull strength of 122 leads was 53.2 grams, with a standard deviation of 12.6 grams (n-1 weighting). A histogram of the data is shown in Figure 2-54. A majority of the pull strength failures occurred in the lead itself, with only one bond lifting from the chip carrier pad at 45.6 grams. Other modes of failure included lifting at the inner bond, bump shearing at the thin film interface, and chipping of the silicon beneath the bump.

2.2.4 Test/Burn-In Process Refinement

All tape designs for semiconductor devices (listed in Table 1-1) utilized as investigative vehicles under this program include provisions for burn-in and functional testing after ILB, as discussed in Paragraph 2.2.5, page 2-54 of Report No. P78-549. The manual punch-out tools shown in Figure 2-55a and 2-55b are used to remove tape metallization shorts, and appropriate wire bonds are added where required. An example of the TCC tape punch-out sequence and resulting interconnections for plating, burn-in testing, and functional testing required for a typical CMOS device, is shown

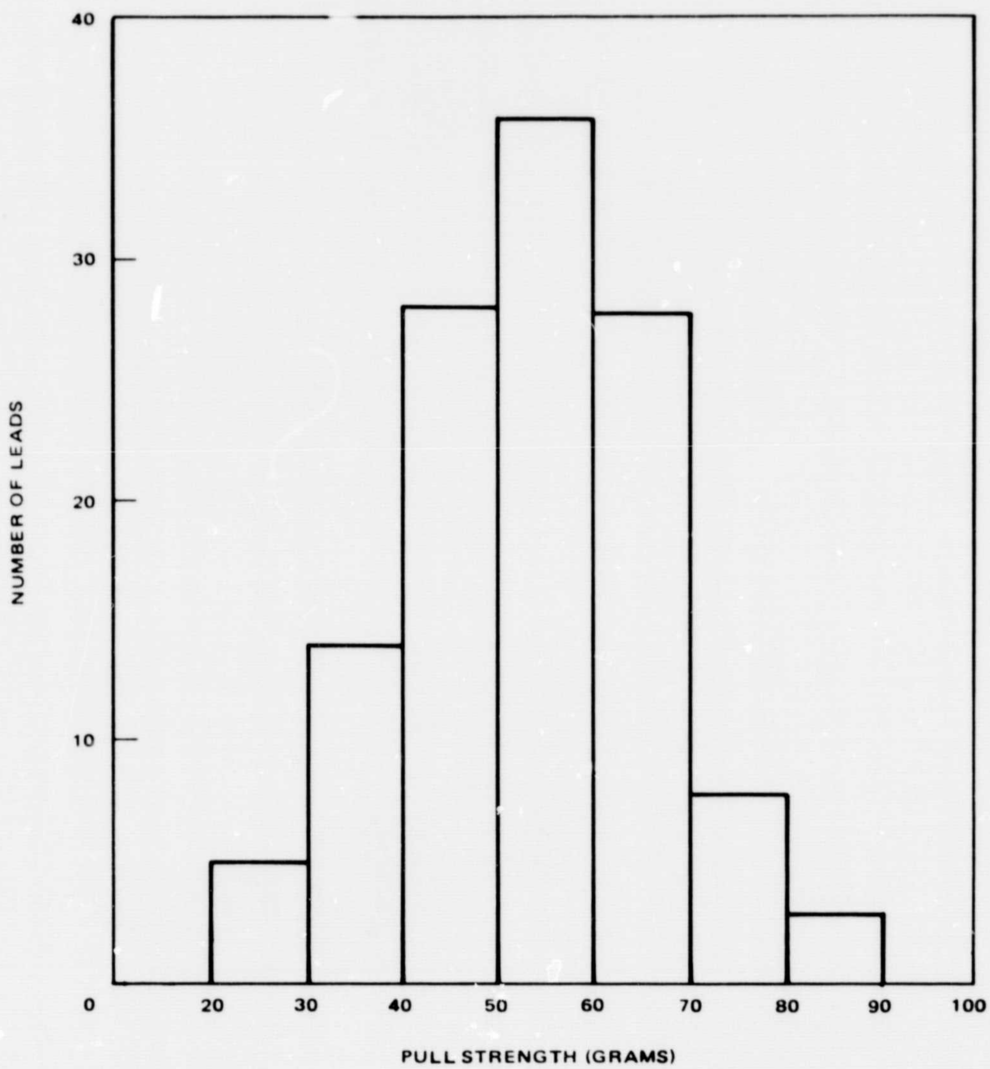
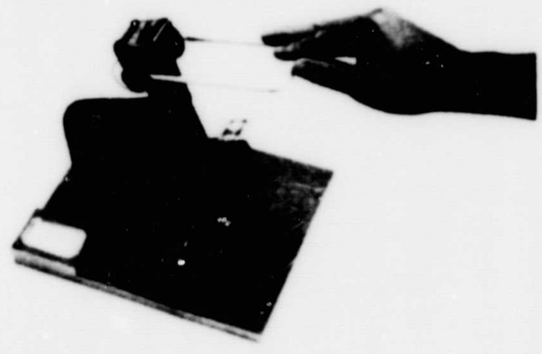


Figure 2-54. Double-bond pull test distribution — 1824 static ram in 24-pad HCC package.



a) TOOL/DIE PUNCH-OUT SET – BENCH-TOP MOUNTING

b) HAND-OPERATED PUNCH-OUT TOOL

Figure 2-55. Manual punch-out tools.

in Table 2-8 and illustrated in Figure 2-56. Time/funding limitations prevented detailed investigation and demonstration of burn-in/functional testing during this Supplementary-Agreement No. -2 time period. Such demonstrations are vital to TCC technology implementation in many hybrid microelectronics applications. For this reason, any follow-on program proposed by Hughes for a potential Supplementary Agreement No. 3 will be based strongly on refining and demonstrating effectiveness related to testing/burn-in aspects of the semiconductor devices mounted on tape chip carriers.

2.2.5 Hybrid Microcircuit Applications

A Hughes-designed Digital Correlator Hybrid Microcircuit (Part No. 1040568) used on an advanced-technology Air Force communications system has been selected for the first TCC process demonstration circuit

TABLE 2-8. EXAMPLE OF TCC TAPE PUNCH-OUT CONNECTION SEQUENCE (TYPE 342 CMOS DIGITAL CORRELATOR)

Condition No.	Description	Pattern Punch-Out and Wire-Bond Connections	Remarks
1.	Original Tape Pattern (Figure 2-23a)	None	All metallization electrically interconnected to permit electrolytic gold plating
2.	Burn-in Tape Pattern (Figure 2-23b)	Positions "A" Punched Out. Wire Bonds "X-X" Connected.	Interconnections remain for burn-in testing. Bias Voltages: 5 volts from outside bar to ground; 10 volts from inside bar to ground.
3.	Functional Test Tape Pattern (Figure 2-23c)	Positions "B" Punched Out. All Wire Bonds Broken.	Probe Pins apply a +5-volt signal between pad 3 and ground (pads 4, 13, 23, and 31); a -5-volt signal between pad 24 and ground; and a +10-volt signal between pads 1/2/20/21/22 and ground. Functional test outputs appear as specified levels at appropriately-numbered clock and signal pads.

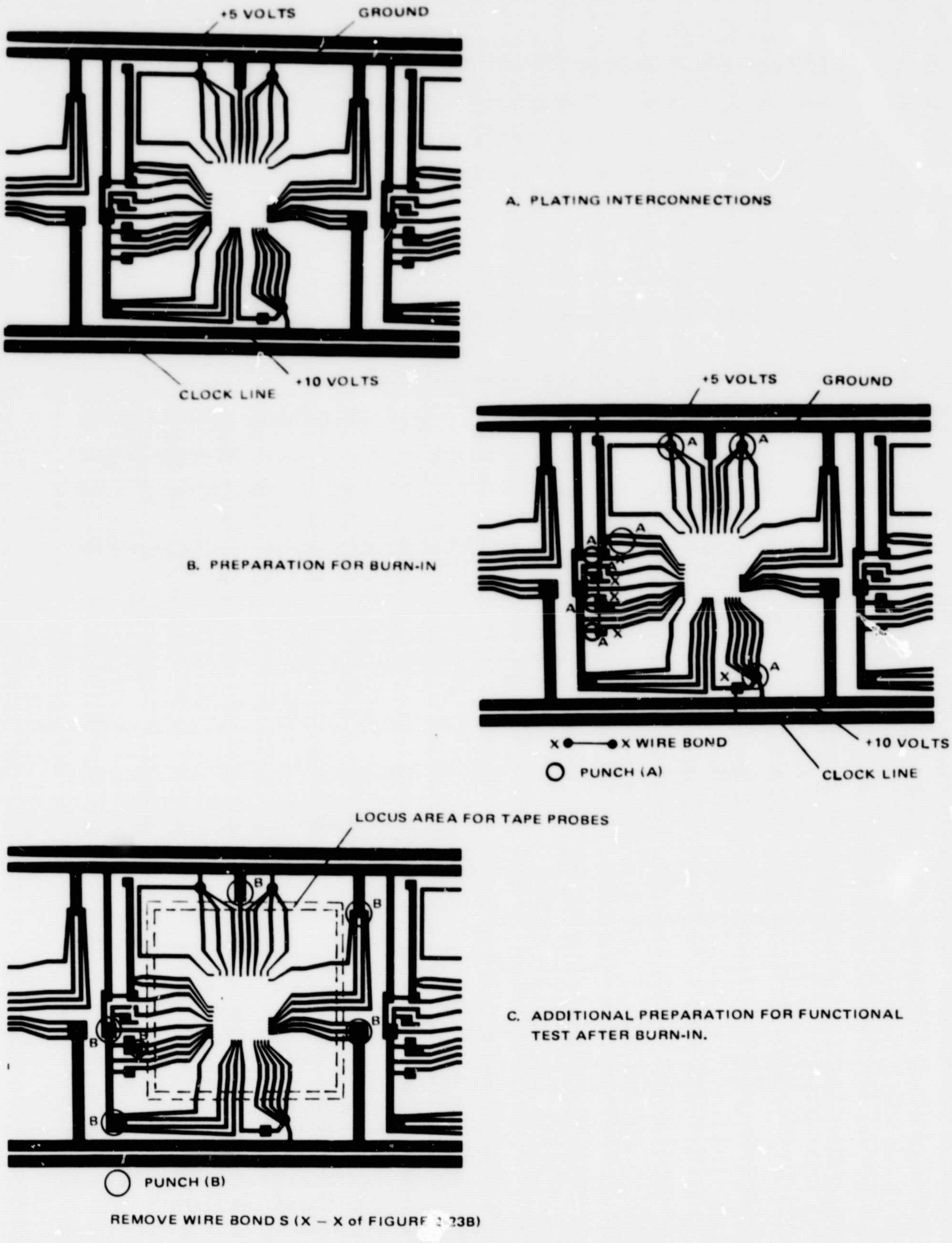


Figure 2-56. Tape Punch-out sequence.

under this program. As shown in the schematic diagram of Figure 2-57, this microcircuit is an excellent example to illustrate the economic need for TCC technology, since a single relatively complex CMOS LSI device (Hughes Type 1037342) is utilized ten times. The conventionally-wire-bonded version, shown in Figure 2-58, currently is being fabricated in the Hughes-Newport Beach SSPD Hybrid Microcircuit Laboratory. First-pass yield rates typically are less than 50 percent, since the chips cannot be characterized functionally in a cost-effective manner prior to microcircuit assembly.

Mechanically-satisfactory Type 342 wafers were bumped during the first six-month time period under Supplementary-Agreement No. 2, as illustrated in Figures 2-59a and 2-59b. The first-iteration patterned tape for this application is shown in Figure 2-60: this same tape is shown superimposed over the matching bumped wafer in Figure 2-61.

Several shortcomings were noted in this first-iteration tape pattern: the longer diagonally-patterned runs were too narrow to achieve the ruggedness of structure normally associated with tape carrier leads. In addition, overlay checkout between the ceramic-based interconnection network and the tape carrier network patterns was insufficient to prevent a minor offset condition. For these reasons, a second-iteration tape carrier layout was designed and fabricated.

The single-layer thin film interconnection network (substrate) currently being utilized (Figure 2-58) has been replaced by an equivalent multilayer thick film network; the two metallization patterns and the dielectric pattern for this network are shown in Figure 2-62; a photograph of the completed multilayer network is shown in Figure 2-63. During the second six-month time period under this program, the ILB, excising, forming, and OLB efforts necessary to fabricate mechanical samples resulted in the tape-mounted digital correlator chips shown in Figure 2-64, and the completed digital correlator unit shown in Figure 2-65. Electrically-operating versions will be fabricated, and comparative yields between the TCC and wired versions will be evaluated during the potential follow-on program which will be proposed by Hughes as Supplementary Agreement No. 3.

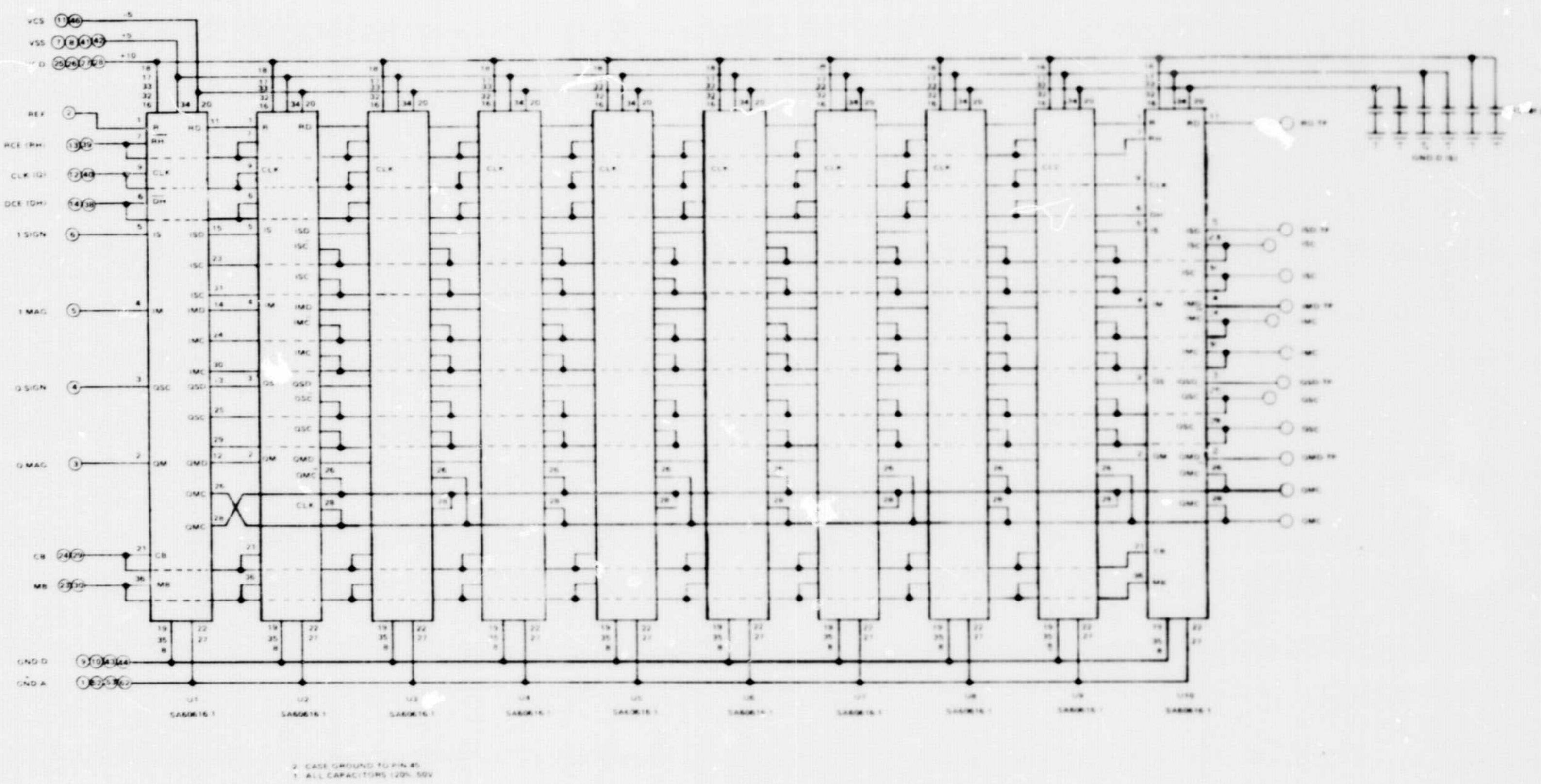


Figure 2-57. Schematic diagram of Type 1040568 digital correlator microcircuit.

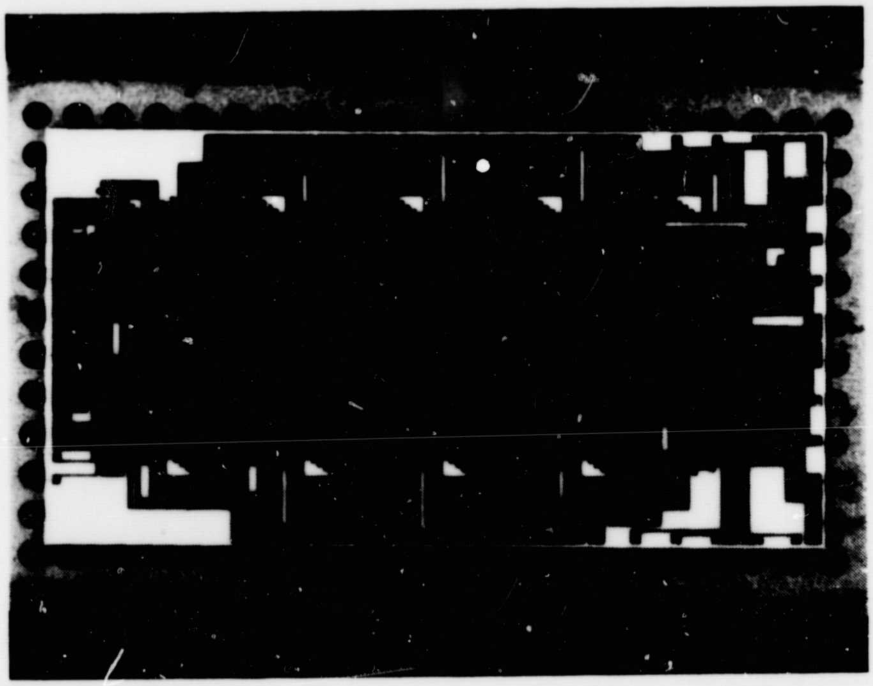
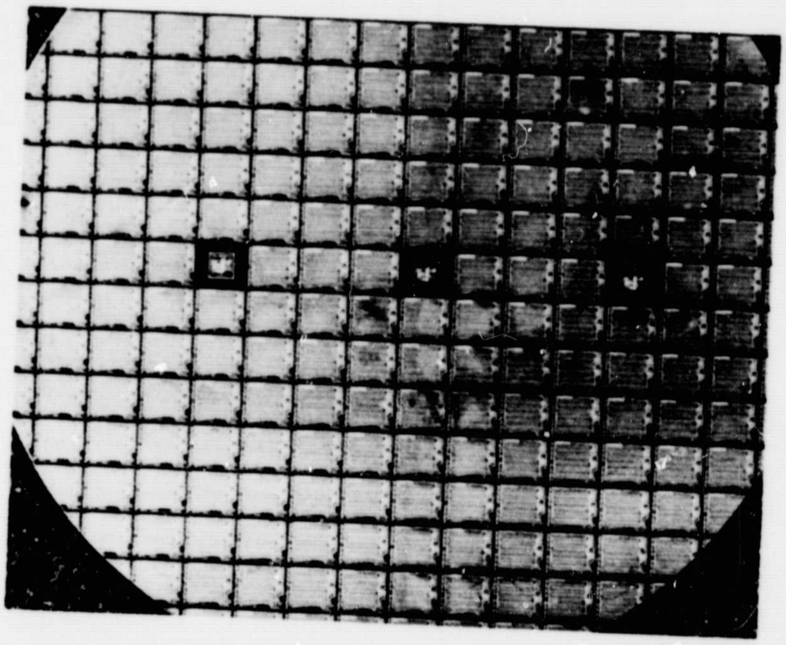


Figure 2-58. Conventionally wire-bonded version of type 1040568 Digital Correlator microcircuit



a. FULL WAFER VIEW

b. CLOSE-UP VIEW

Figure 2-59. Bumped Type 342 CMOS digital correlator wafer.

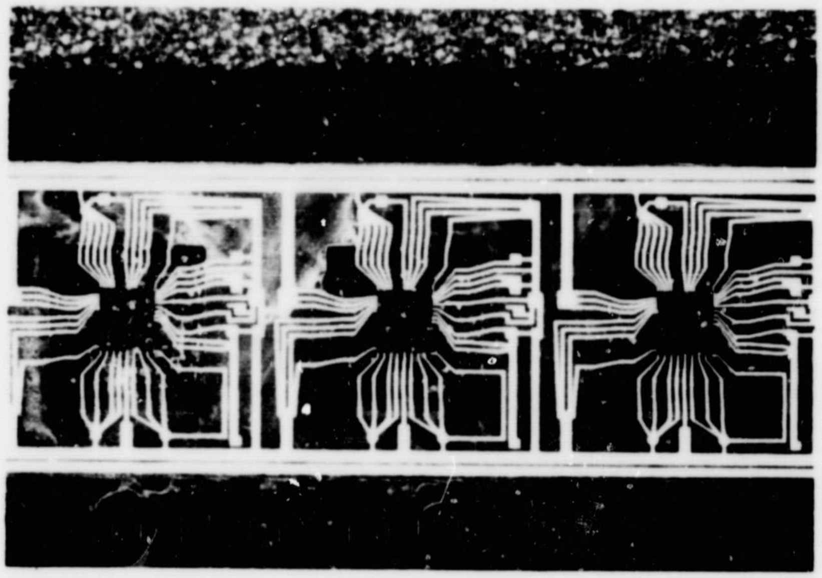


Figure 2-60. Tape carrier patterned for Type 342 LSI devices.

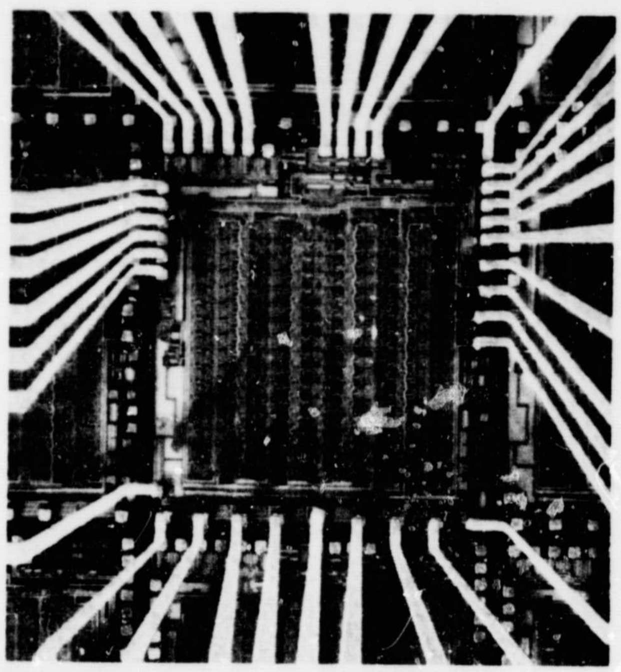
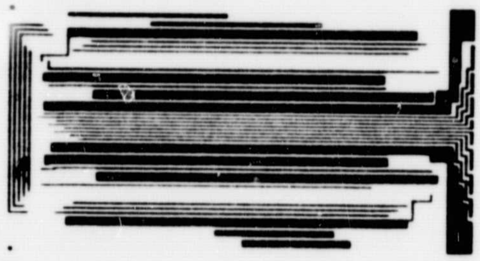
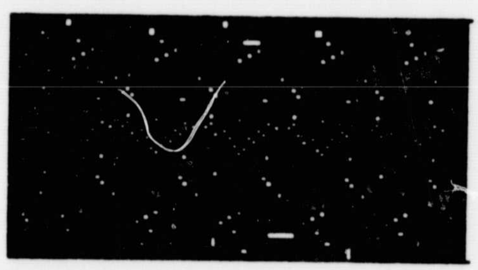


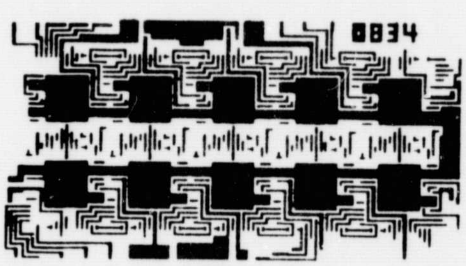
Figure 2-61. Tape carrier for Type 342 devices shown superimposed over matching bumped wafer



FIRST CONDUCTOR



DIELECTRIC



SECOND CONDUCTOR

Figure 2-62. Metallization/dielectric patterns for Type 1040568 digital correlator multilayer thick film interconnection network.

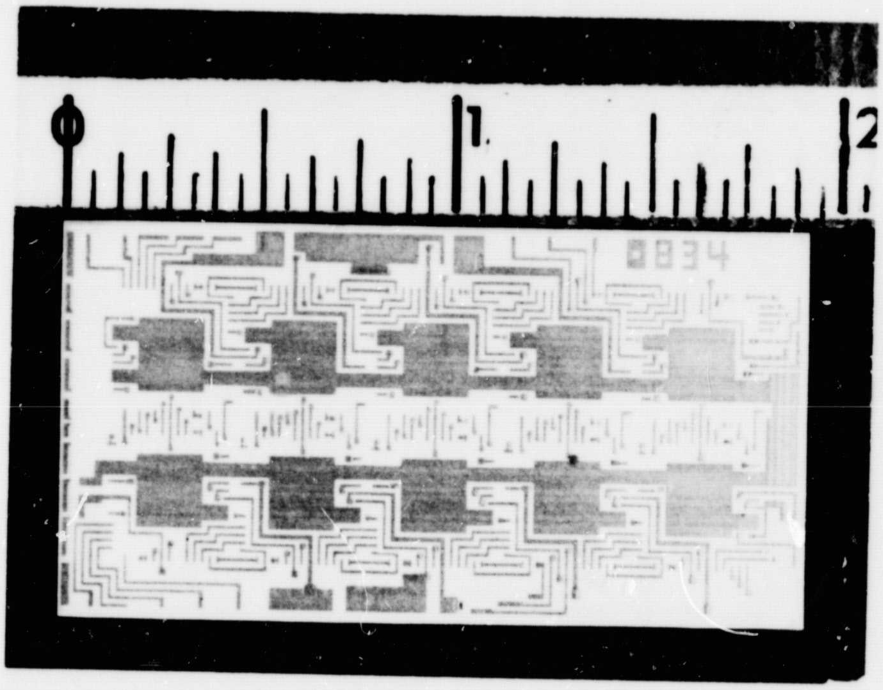
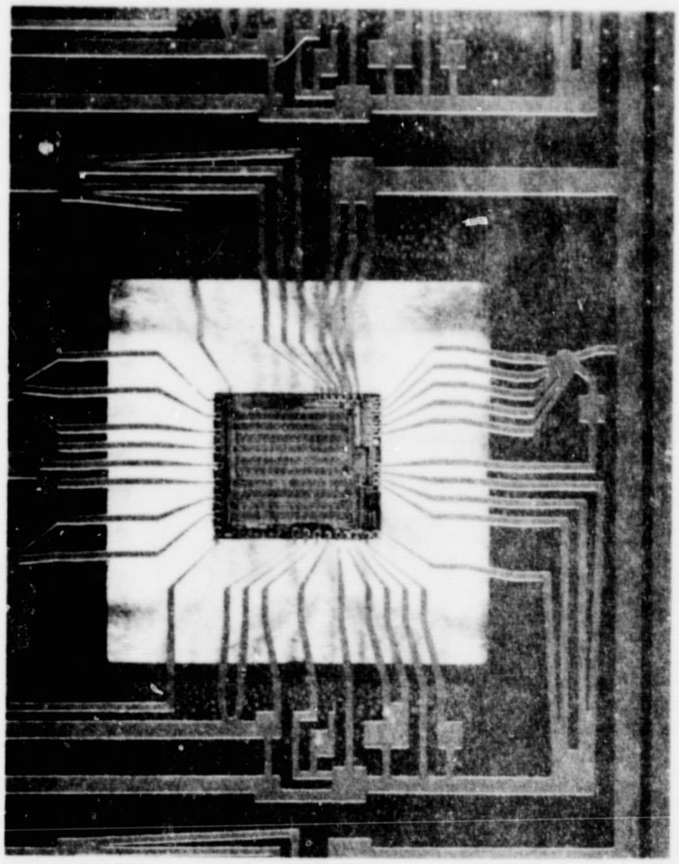


Figure 2-63. Screened/Fired multilayer network for digital correlator.



a. TAPE MOUNTED CHIP

b. CLOSE-UP VIEW

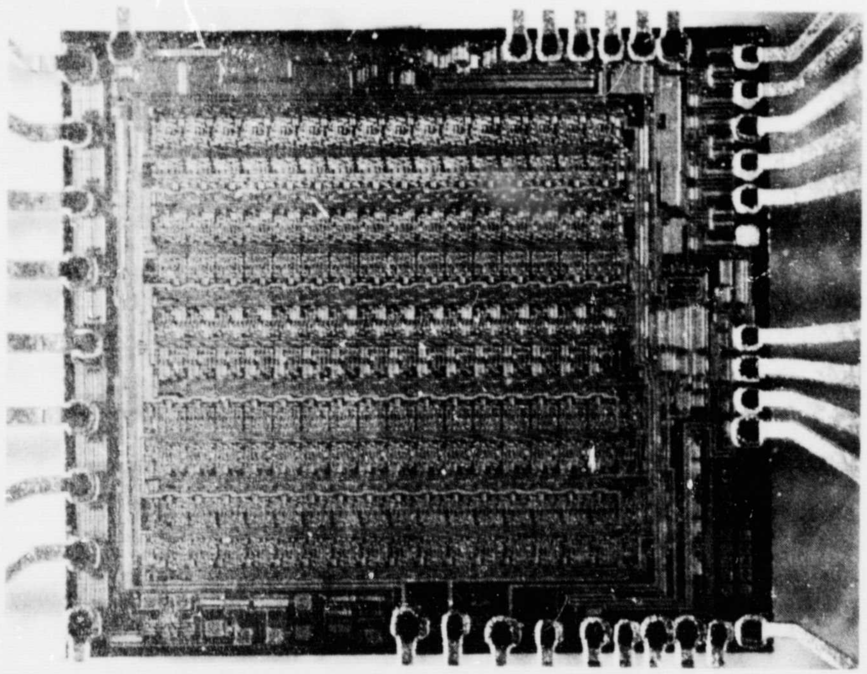
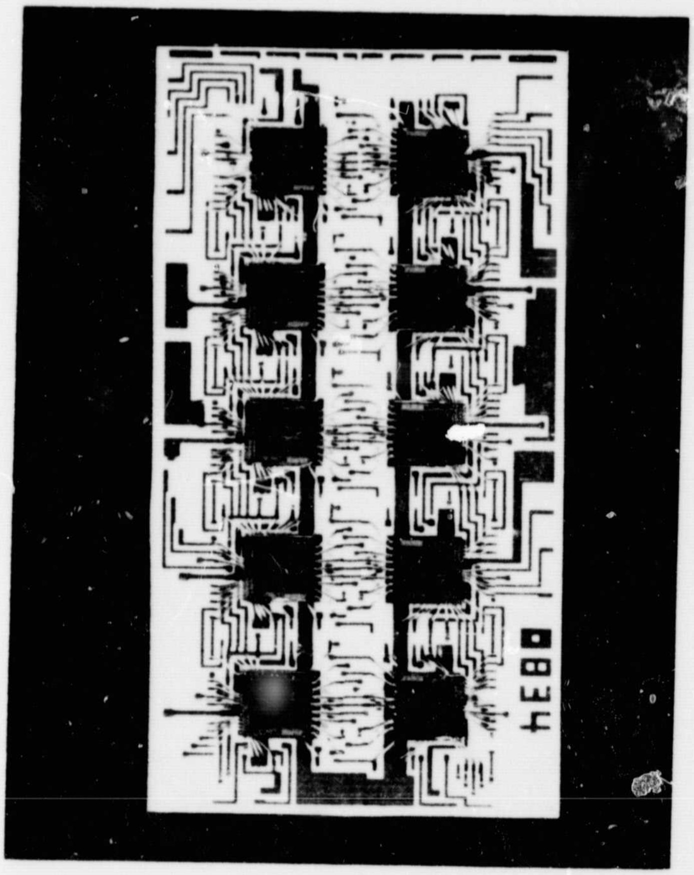
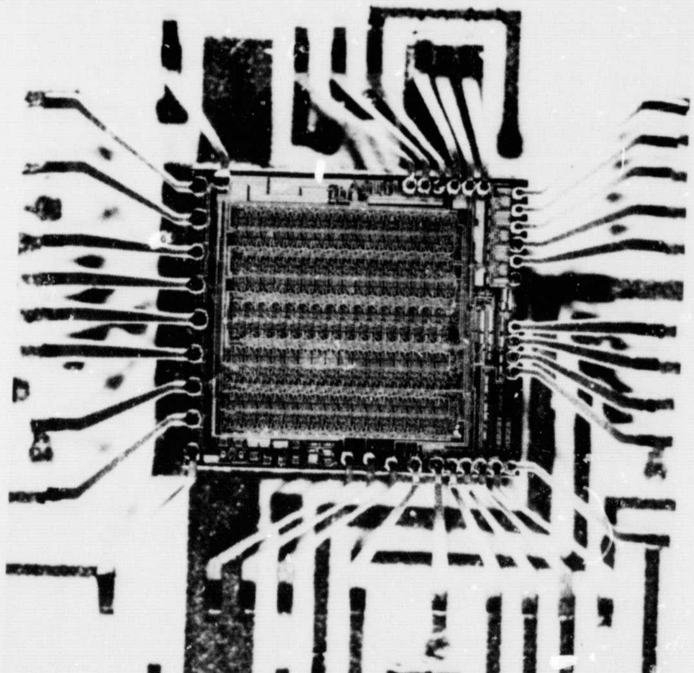


Figure 2-64. Tape-mounted digital correlator chip.



a. OVERALL VIEW



b. CLOSE UP VIEW

ORIGINAL PAGE IS
OF POOR QUALITY

Figure 2-65. Completed digital correlator hybrid microcircuit (mechanical).

2.2.6 STAR Wafer Application

During November, 1978 telephone conversations, cognizant MSFC personnel agreed to supply mechanical wafers and pad location masks so that Hughes wafer bumping activities on STAR devices could be initiated.

For the initial baseline concept, it was envisioned that 84-pad hermetic chip carriers (HCCs) would be used. The layout drawing of this HCC package (Figure 2-66) shows a 0.470-inch square cavity.

It was planned that gold-bumped STAR devices were to be bonded eutectically within the HCC package cavity during the Supplementary-Agreement-No.-2 time period, using either gold-silicon or gold-germanium preforms; after which one-mil gold wire interconnections were to have been made (both chip-to-chip and chip-to-package bonding shelf) by means of the Hughes Model 1460 Semi-Automatic Wire Bonder.

Eight 1.5-inch-diameter 38-pad STAR mechanical wafers were received from MFSC on 12 January 1979, together with metallization masks on 2-inch x 2-inch glass plates. During a January, 1979 visit by MSFC personnel to Hughes-Newport Beach, program progress was discussed. It was pointed out that 3-inch x 3-inch masks are required to match currently-used Hughes aligners for wafer bumping, and that these masks should include pad metallization locations/sizes only; the scribe lines and/or actual interconnection metallization which appeared on the masks received from MSFC were to be deleted to avoid excess gold plating in unwanted areas.

A second shipment comprising 3-inch x 3-inch masks was received on 22 January 1979, but these also included the scribe lines/metallization patterns. During subsequent telephone conferences with cognizant MSFC personnel, it was determined that the correct masks indeed were available; and that they would be shipped within several days. In the meantime, the wafers themselves had been sputter-coated with tungsten-titanium/gold. They were to be dry-resist-laminated, and then placed on "hold" pending receipt of the proper bump plating masks, expected early in February.

Corrected pad masks for the 38-pad STAR mechanical wafers were received from MSFC on 5 February 1979. The eight 1.5-inch wafers which had been received from MSFC on 12 January, and coated at Hughes with tungsten-titanium/gold, developed micro-cracks, and some actually were

C-2

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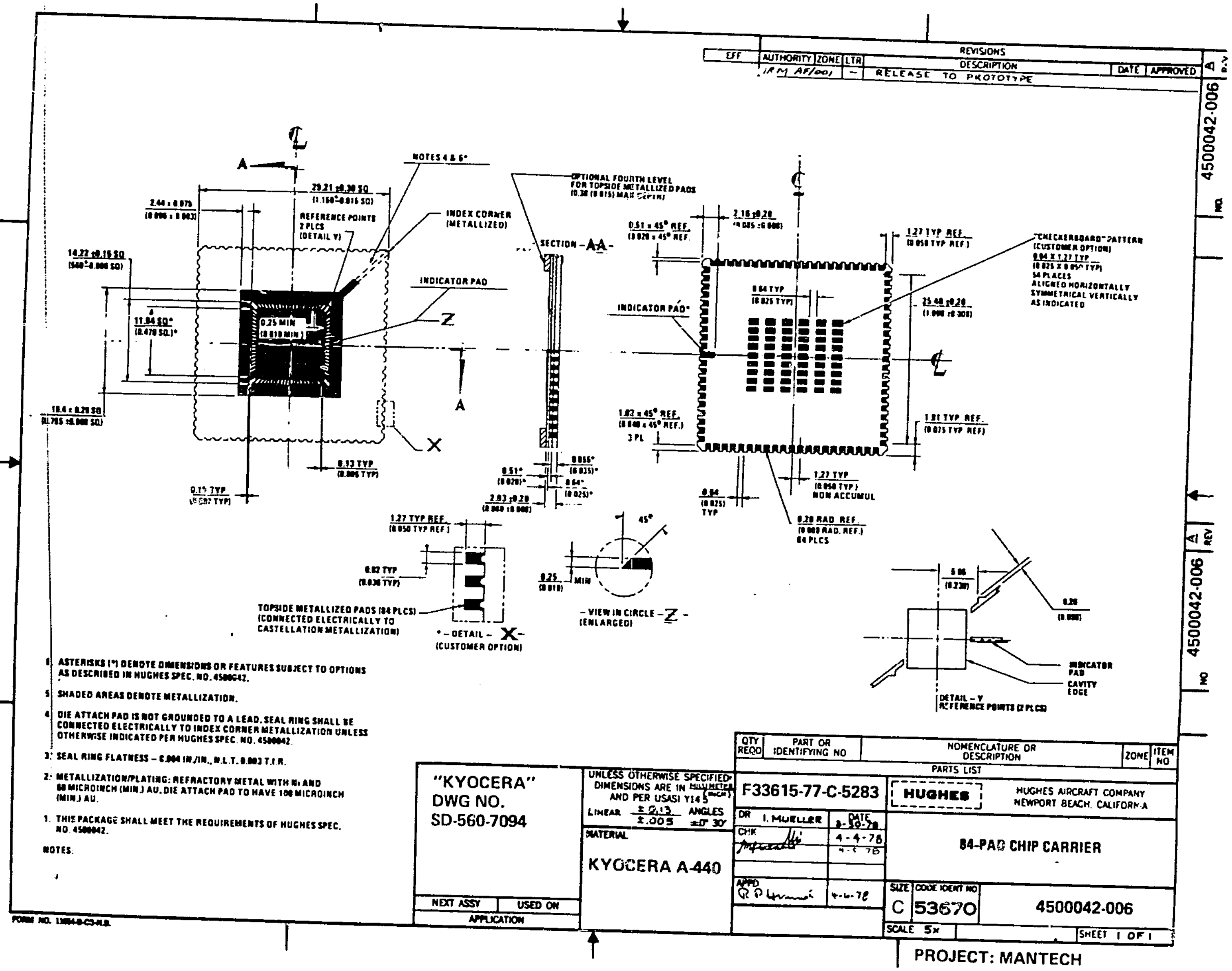
C-2



PROJECT: MANTECH

Figure 2-66. Outline drawing of 84-pad HCC package (Hughes Type 4500042-006).

broken. Others broke after dry-resist lamination; a process which generally does not cause wafer breakage. The eight-to-ten-mil nominal thickness of these 1.5-inch-diameter wafers apparently contributes to their relative brittleness in comparison to the 2-1/4-inch, 3-inch, and/or 4-inch wafers normally subjected to the wafer bumping process (nominally 12-to-20-mils in thickness).

Attempts were made to align larger wafer portions, so as to yield initial bumped chips. This proved to be impractical however, and additional wafers were requested from MSFC.

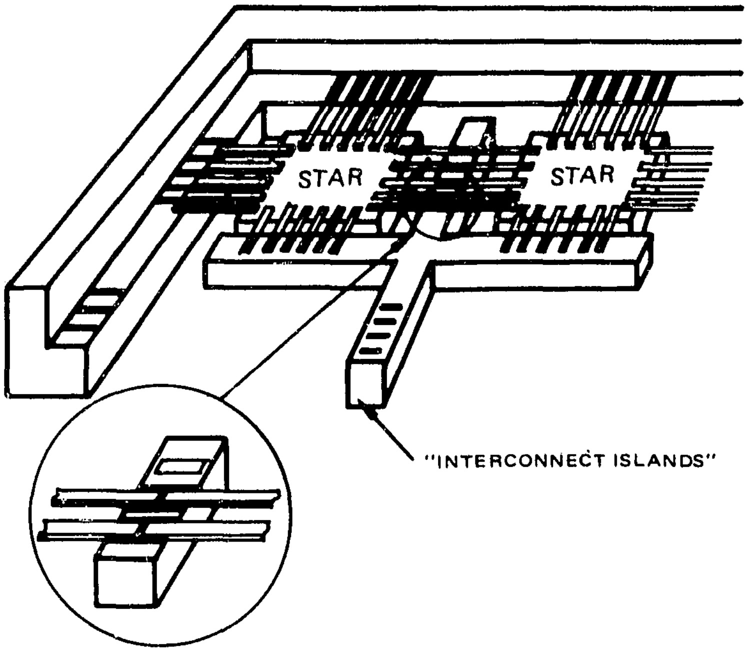
These additional mechanical wafers, received during April, 1979, were handled with extra precautions to preclude breakage. Bumping of these wafers has been initiated; completion will be scheduled to assure mechanical checkout prior to receipt of electrically-operating wafers during potential follow-on efforts to be proposed under Supplementary Agreement No. 3.

Time and funding considerations have precluded further effort related to STAR devices under Supplementary Agreement No. 2. In connection with potential follow-on efforts to be proposed for Supplementary Agreement No. 3, the wafers will be sawed (using processing discussed in Report No. P78-549[1], Paragraph 2.2.2, page 2-43), and individual chips will be bonded eutectically within the 84-pad hermetic chip carrier as discussed above. Thermosonically-bonded one-mil gold wire will form interconnections between chips, and between the chips and package. The gold bumps on the chips will permit monometallic (gold-to-gold) interconnection bonding; this will eliminate the possibility of gold-aluminum intermetallic formation and associated problems. The wafers will be checked out for electrical continuity (open/shorts) after bumping and before assembly.

Wafer dicing and assembly will take place after these preliminary tests have been completed, so that testing may be performed at the package level.

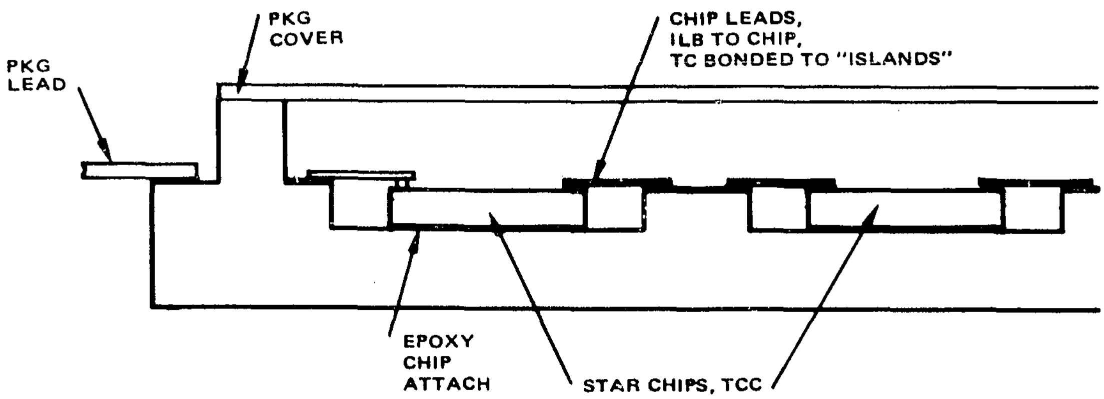
2.2.7 Improved Packaging Recommendations

A method for improved packaging of bumped STAR chips from tape carriers will be utilized under potential follow-on programs to be proposed by Hughes. As indicated in Figure 2-67, this approach involves hermetic

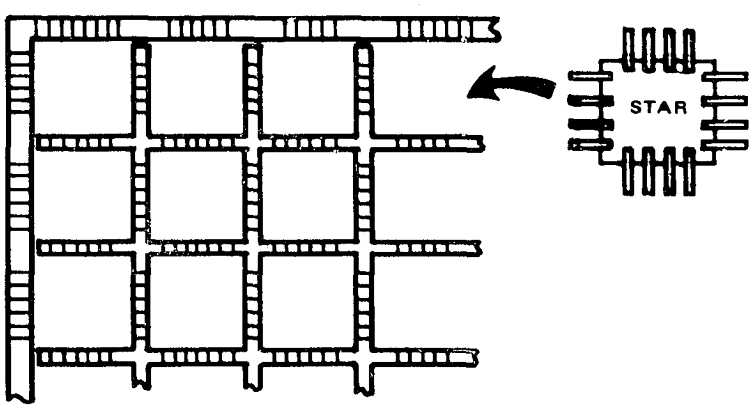


- IC's ARE BUMPED, PLACED ON TAPE, TESTED, SCREENED.
- GOOD IC's (ON TAPE) ARE EXCISED, PICKED AND PLACED INTO PACKAGE.
- STANDARD INTERCONNECT PACKAGES CONTAIN "INTERCONNECT ISLANDS" TO ACCOMMODATE ADJACENT TAPED IC's.
- STANDARD PACKAGES TO BE AVAILABLE IN STEPS SUCH AS 2 X 2, 3 X 3, 4 X 4, ETC.

a. Detailed top view



b. Cross-section, STAR standard packaging



c. Top view of STAR array package

Figure 2-67. Proposed STAR standard packaging.

chip carriers which will be prepared by the addition of special interconnect islands. These ceramic islands, previously metallized with interconnection pads and brazed within the package cavities, will serve as receptors for the outer-lead bonding of pretested "spider" assemblies after they have been excised from tape carriers.

Approaches such as this will aid in bringing about practical applications for the STAR concept under development at MSFS. Further Hughes proposals will address problems of this nature; packaging approaches such as this will provide viable solutions to problems involving cost-factors determination related to electronic subsystems utilizing LSI microcircuits such as STAR.

APPENDIX A
REFERENCES

1. "Design, Processing and Testing of LSI Arrays, Hybrid Microelectronics Task", Final Report, Contract No. NAS8-32607, August, 1978. (HAC Ref. No. E07711)

2. Design, Processing and Testing of LSI Arrays - Hybrid Microelectronics Task, Semiannual Report (March, 1979), NASA Contract NAS8-32607 (HAC Ref. No. E07711); paragraph 2.2.1, pages 2-3 through 2-15.

3. TIC No. 7631.10/187, Leadless Ceramic Chip Carrier Cost Analysis.

APPENDIX B

HYBRID MICROELECTRONICS – COMPUTER PROGRAM TO CALCULATE SINGLE VALUED HYBRID COSTS

```
C        "HYBRID MICROELECTRONICS: Cost Modeling Program"
         IMPLICIT REAL(K,L)
C        This program computes the following values and
C        outputs them at the terminal and into the data
C        file HYBRID.DAT:
10       FORMAT (/,' Complexity factor CC = ', F4.2,/)
20       FORMAT (' Substrate fabrication cost C''SP
         2 = $ ', F6.2,/)
30       FORMAT (' Assembly cost C''AT
         2 = $ ', F8.2,/)
40       FORMAT (' Recurring material cost CM = $ ', F6.2,/)
50       FORMAT (' Total hybrid cost = $ ', F8.2,/)
60       FORMAT (' Tape chip carrier cost differential
         2CTCC = $ ', F8.2,/)
70       FORMAT (' Total hybrid cost with tape chip
         2carrier = $ ', F8.2)
C
80       FORMAT (/,5X,' HYBRID MICROELECTRONICS MANUFACTURE: ')
90       FORMAT (' Add computations based on tape chip carrier
         2 (TCC) technology? ',/,5X, ' (YES or NO): ', $)
100      FORMAT (5X,' Alternate case: Tape Chip Carrier ',/)
110      FORMAT (5X,' Alternate case selected: ',/,5X,
         2' Effect of tape chip carrier (TCC) technology ',
         3/,5X,' on hybrid manufacturing cost: ',/)
120      FORMAT (A5)
130      FORMAT (' TCC included ')
140      FORMAT (' TCC not included ')
         TYPE 90
         ACCEPT 120,CASE
         IF (CASE.EQ.'YES')TYPE 130
         IF (CASE.EQ.'NO')TYPE 140
C
C        I.  G E N E R A L   C O S T   F A C T O R S
         BETA = -0.4      ! Production volume exponent
         GAMMA=2.5 ! Production facility factor
         P1=9 !  Non-recurring developmental costs :
C                developmental-to-manufacturing cost ratio
         P2=3 !  Non-recurring manufacturing costs:
C                non-recurring to recurring manuf. cost ratio
         V=10     ! Number of hybrids produced per year
         WR=12            ! Wage rate, dollars
C
C        II.  S U B S T R A T E   F A B R I C A T I O N
C        VALUES OF CONSTANTS AND PARAMETERS :
C        (STDH = Standard hours)
C             Constants:
         COS=30          ! Substrate material, dollars
         COE=0.124       ! Circuit processing, STDH
         KT=0.205        ! Resistor trimming, STDH x sq. in.
         KQC=0.072       ! Resistor trimming, STDH
         KPRQC=0.072     ! K'QC, Quality control (QC) inspection
C                          factor, non-dimensional
C             Parameters:
         APR =1   ! a', Number of reworks before resistor trimming
         BPR =0   ! b', Number of reworks after resistor trimming
         AREA = 1.3125    ! Substrate area, square inches
         NC=45    ! Total number of chips
         DELTAC = NC/AREA         ! No. of chips/square inch
         NR=30    ! Total number of resistors
         DELTAR = NR/AREA         ! No. of resistors/sq. in.
```

```
      DELTSR=5.4E-4  ! Delta-SR, area of resistor hybrid area
      TR=5           ! Inverse of tolerance
      SZ=0.5         ! Hybrid size factor
      DELTAP = 16     ! Number of pads on IC
      DEPMAX=14      ! Delta-Pmax, maximum no. of pads on IC
      LW=0.75 ! Line width factor
      CC=.0055*(DELTAC+DELTAR)+.0071*DEPMAX**1.1
C     (Hybrid complexity factor [Medium complexity])
C     FABRICATION STEPS:
      CS = COS*SZ       ! Substrate material cost
      CP = COE*CC*LW    ! Circuit photoetching processing
      CQC = KQC*CC*SZ           ! QC inspection cost (I)
      CPRQC = KPRQC*CC*SZ      ! QC inspection cost (II)
      CU = 0.024       ! Cutting substrate to size
      CRT = KT*DELTSR*DELTAR*TR        ! Resistor trimming
C     Substrate fabrication cost, volume-independent:
      CSP = (1+APR+BPR)*(CS+(CP+CPRQC)*WR)
     2       +(1+BPR)*(CU+CRT+CQC)*WR
C     Substrate fabrication cost C'SP, volume-dependent:
      CPRSP = CSP*(P1+P2+1)*CC*GAMMA*V**BETA
C
C     III. A S S E M B L Y   A N D   T E S T I N G
C     VALUES OF CONSTANTS AND PARAMETERS :
C          Constants:
      COPT=0.033       ! Pre-tin, STDH
      ALPHA =9.5E-3    ! Chip bonding, STDH
      B = 6.6E-4       ! b,  Wire bonding constant, STDH
      D=0.0033         ! d, Non-destructive pull test, STDH
      KQC1=0.086       ! Pre-seal QC inspection, STDH
      G=0.95           ! g, Pre-seal electrical test, STDH
      GPR=1.2          ! g', Pre-seal troubleshooting, STDH
      H=0.025          ! h, Pre-seal rework, STDH
      KQC2=0.51        ! Pre-seal QC inspection, STDH
      L=0.186          ! Proportional constant, sealing, STDH
      GPR2=1.38        ! g", Post-seal troubleshooting, STDH
      HPR=0.044        ! h', Rework after sealing, STDH
      KQC3=0.02        ! Final QC inspection factor, STDH
C          Parameters:
      NTRJ=480! Total no. of transistor junctions of ICs
      NTRD=13 ! Total number of transistors and diodes
      NCAP=20 ! Total number of capacitors
      NCIC=12  ! Total number of ICs
      NWB=640 ! Total number of bonds
      TY=1    ! Package type (Butterfly = 2; HAC-PAC = 1)
      Q=10000 ! Number of packages per lot
      CLPR=1.70 ! C'L, Average cost of a package lid, dollars
      N = 10  ! n, Number of reworks before sealing
      NPR = 1 ! n', Number of reworks after sealing
      M=1        ! m, Die attachment factor
C                 (1 = epoxy; 2 = molytab)
      F=0.4      ! f, Fraction of other connections
      R=1      ! r, Reliability level factor
      AVNTRJ=40 ! Average no. of transistor junctions/chips
      G1=0.1  ! g1, Fraction of chips reworked before sealing
      G2=0.05 ! g2, Fraction of bonds reworked before sealing
      G1PR=0.02! g'1, Fraction of chips reworked after sealing
      G2PR=0.004!g'2, Fraction of bonds reworked after sealing
      CLR=0.2 ! Rework due to lid substitution, STDH
      CTT=0.22! Acceptance test, STDH
C     ASSEMBLY STEPS:
```

```
C             Pre-tinning cost:
      CPT = SZ*COPT
C             Substrate bonding:
      CBS = 0.12
C             Chip bonding cost:
      CBC = M*ALPHA*NC
C             Wire bonding cost:
      CWB = B*((DELTAP*NCIC+2*(NTRD+NCAP))*(1+F))
C             Non-destructive pull test:
      CND = D*(R*NWB)
C             Visual QC inspection before sealing:
      CQC1 = KQC1*CC*SZ
C             Electrical testing before sealing:
      CEPS = N*G*AVNTRJ**0.1*CC
C             Troubleshooting before sealing:
      CTROB = N*GPR*AVNTRJ**0.1*CC
C             Reworking before sealing:
      CRWB = N*H*(G1*NC+G2*NWB)
C             2nd visual QC inspection before sealing:
      CQC2 = KQC2*CC*SZ
C             Sealing cost:
      CSL = L*SZ
C             Acceptance test after sealing:
      CACT = R*CTT
C             Troubleshooting after sealing:
      CTROA = NPR*GPR2*AVNTRJ**0.1*CC
C             Reworking after sealing:
      CRWA = NPR*(HPR*(G1PR*NC+G2PR*NWB)+CLR)
C             Final quality control inspection:
      CQC3 = KQC3*SZ
C             Other steps:
      CO = 0.25
C     Assembly cost, volume-independent:
      CAT = (CPT+CBS+CBC+CWB+CND+CQC1+CEPS+CTROB+CRWB
     2      +CQC2+CSL+CACT+CTROA+CRWA+CQC3+CO)*WR
C     Assembly cost C'AT, volume-dependent:
      CPRAT = CAT*(P1+P2+1)*CC*GAMMA*V**BETA
C
C     IV.  R E C U R R I N G   M A T E R I A L   C O S T
      CP=23*TY*SZ*EXP(-7E-6*Q)! Package cost
      CCC=0.13*NTRJ+0.80*NTRD ! Chip cost
     2   +1.6*NCAP
      CL=NPR*CLPR              ! Package lid cost
      CM=CP+CCC+CL
      IF (CASE.EQ.'NO')GO TO 200
C
C     V. TAPE CHIP CARRIER COST FACTORS
C             Substitutions:
C     CEPS >> (0.7)CEPS
C     CRWB >> (0.6)CRWB
C     CBC  >> (0.9)CBC
C     CWB  >> (0.5)CWB
C     CND  >> (0.3)CND
      U = 2.75E-2       ! u, Chip testing constant, STDH
      CTC = U*NCIC      ! Chip testing cost with TCC
      UB = 9.5E-2       ! uB, Cost of bumping one chip, $
      CBP = UB*NCIC     ! Bumping cost, dollars
C     Cost differential of tape chip carrier:
      CTCC = (((0.7-1)*CEPS+(0.6-1)*CRWB+(0.9-1)*CBC
     2      +(0.5-1)*CWB+(0.3-1)*CND+CTC)*WR+CPB)
```

```
     3       *(P1+P2+1)*V**BETA
C
C          VI. T O T A L   H Y B R I D   C O S T
           CH=CTCC+CPRSP+CPRAT      ! With TCC
200        COST=CM+CPRSP+CPRAT
C
           TYPE 10,CC
           TYPE 20,CPRSP
           TYPE 30,CPRAT
           TYPE 40,CM
           TYPE 50,COST
           OPEN (UNIT=21,DEVICE=DSK,FILE='HYBRID.DAT')
           WRITE(21,80)
           WRITE(21,10)CC
           WRITE(21,20)CPRSP
           WRITE(21,30)CPRAT
           WRITE(21,40)CM
           WRITE(21,50)COST
           IF(CASE.EQ.'NO')GO TO 300
           TYPE 100
           TYPE 60,CTCC
           TYPE 70,CH
           WRITE(21,110)
           WRITE(21,60)CTCC
           WRITE(21,70)CH
300        END
```

APPENDIX C

HYBRID MICROELECTRONICS – COMPUTER PROGRAM TO CALCULATE HYBRID COST MATRICES FOR THE GENERATION OF COST SURFACES

```
C       "HYBRID MICROELECTRONICS: matrix Program"
C       This program generates a matrix to be used to plot
C       hybrid microelectronics fabrication costs as a function
C       of two variables (selected fabrication cost factors)
C       on a 3D surface using the Thermal Process of the
C       Analysis subsystem of CAD.
C       (Fortran subroutine called: DCDFIL; execute command:
C       EXECUTE HYBMAT.FOR,REL:SUB/LIB)
        IMPLICIT REAL(K,L)
        INTEGER IFLU,I,J
        DIMENSION IPPN(3), FNAME(5)
        DIMENSION COST(50,50)
        REAL*8 FILNAM
        DATA IFLU/20/
10      FORMAT (/,5X,' HYBRID MICROELECTRONICS MANUFACTURE:
        2Matrix Generation ')
20      FORMAT (' Enter output file name : ', $)
30      FORMAT (5A5)
40      FORMAT ('!TEST')
50      FORMAT (50G)
60      FORMAT ('*')
        TYPE 10
        TYPE 20
        ACCEPT 30, FNAME
        CALL DCDFIL (FNAME, 'DAT', FILNAM, IPPN)
        OPEN (UNIT=IFLU, ACCESS='SEQOUT', MODE='ASCII',
        1FILE=FILNAM, DIRECTORY=IPPN, DISPOSE='SAVE')
        WRITE(IFLU,40)
        DO 100 I=1,50
        DO 100 J=1,50
        NC=5*I
        V=J*2
C       I.  G E N E R A L   C O S T   F A C T O R S
        BETA = -0.4      ! Production volume exponent
        GAMMA=2.5 ! Production facility factor
        P1=9 !  Non-recurring developmental costs :
C                developmental-to-manufacturing cost ratio
        P2=3 !  Non-recurring manufacturing costs:
C                non-recurring to recurring manuf. cost ratio
        WR=12            ! Wage rate, dollars
C
C       II.  S U B S T R A T E   F A B R I C A T I O N
C       VALUES OF CONSTANTS AND PARAMETERS :
C       (STDH = Standard hours)
C            Constants:
        COS=30          ! Substrate material, dollars
        COE=0.124       ! Circuit processing, STDH
        KT=0.205        ! Resistor trimming, STDH x sq. in.
        KQC=0.072       ! Resistor trimming, STDH
        KPRQC=0.072     ! K'QC, Quality control (QC) inspection
C                         factor, non-dimensional
C            Parameters:
        APR =1  ! a', Number of reworks before resistor trimming
        BPR =0  ! b', Number of reworks after resistor trimming
        AREA = 1.3125    ! Substrate area, square inches
C       NC=Total number of chips (matrix element)
        DELTAC = NC/AREA         ! No. of chips/square inch
        NR=30           ! Total number of resistors
        DELTAR = NR/AREA         ! No. of resistors/sq. in.
        DELTSR=5.4E-4   ! Delta-SR, area of resistor hybrid area
```

```
      TR=5            ! Inverse of tolerance
      SZ=0.5          ! Hybrid size factor
      DELTAP = 16     ! Number of pads on IC
      DEPMAX=14       ! Delta-Pmax, maximum no. of pads on IC
      LW=0.75 ! Line width factor
      CC=.0055*(DELTAC+DELTAR)+.0071*DEPMAX**1.1
C     (Hybrid complexity factor [Medium complexity])
C     FABRICATION STEPS:
      CS = COS*SZ         ! Substrate material cost
      CP = COE*CC*LW  ! Circuit photoetching processing
      CQC = KQC*CC*SZ            ! QC inspection cost (I)
      CPRQC = KPRQC*CC*SZ        ! QC inspection cost (II)
      CU = 0.024        ! Cutting substrate to size
      CRT = KT*DELTSR*DELTAR*TR         ! Resistor trimming
C     Substrate fabrication cost, volume-independent:
      CSP = (1+APR+BPR)*(CS+(CP+CPRQC)*W1)
     2        +(1+BPR)*(CU+CRT+CQC)*W2
C     Substrate fabrication cost C'SP, volume-dependent:
      CPRSP = CSP*(P1+P2+1)*CC*GAMMA*V**BETA
C
C     III. A S S E M B L Y   A N D   T E S T I N G
C     VALUES OF CONSTANTS AND PARAMETERS :
C          Constants:
      COPT=0.033        ! Pre-tin, STDH
      ALPHA =9.5E-3     ! Chip bonding, STDH
      B = 6.6E-4        ! b, wire bonding constant, STDH
      D=0.0033          ! d, Non-destructive pull test, STDH
      KQC1=0.069        ! Pre-seal QC inspection, STDH
      G=0.95            ! g, Pre-seal electrical test, STDH
      GPR=1.2           ! g', Pre-seal troubleshooting, STDH
      H=0.025           ! h, Pre-seal rework, STDH
      KQC2=0.51         ! Pre-seal QC inspection, STDH
      L=0.166           ! Proportional constant, sealing, STDH
      GPR2=1.38         ! g", Post-seal troubleshooting, STDH
      HPR=0.044         ! h', Rework after sealing, STDH
      KQC3=0.02         ! Final QC inspection factor, STDH
C          Parameters:
      NTRJ=480! Total no. of transistor junctions of ICs
      NTRD=13 ! Total number of transistors and diodes
      NCAP=20 ! Total number of capacitors
      NCIC=12   ! Total number of ICs
      NWB=640 ! Total number of bonds
      TY=1     ! Package type (Butterfly = 2; HAC-PAC = 1)
      Q=10000 ! Number of packages per lot
      CLPR=1.70 ! C'L, Average cost of a package lid, dollars
      N = 10   ! n, Number of reworks before sealing
      NPR = 1 ! n', Number of reworks after sealing
      M=1          ! m, Die attachment factor
C              (1 = epoxy; 2 = molytab)
      F=0.4        ! f, Fraction of other connections
      R=1      ! r, Reliability level factor
      AVNTRJ=40 ! Average no. of transistor junctions/chips
      G1=0.1  ! g1, Fraction of chips reworked before sealing
      G2=0.05 ! g2, Fraction of bonds reworked before sealing
      G1PR=0.02! g'1, Fraction of chips reworked after sealing
      G2PR=0.004!g'2, Fraction of bonds reworked after sealing
      CLR=0.2 ! Rework due to lid substitution, STDH
      CTT=0.22! Acceptance test, STDH
C     ASSEMBLY STEPS:
C           Pre-tinning cost:
```

```
      CPT = SZ*COPT
C           Substrate bonding:
      CBS = 0.12
C           Chip bonding cost:
      CBC = M*ALPHA*NC
C           Wire bonding cost:
      CWB = H*((DELTAP*NCIC+2*(NTRU+NCAP))*(1+F))
C           Non-destructive pull test:
      CND = D*(P*NWP)
C           Visual QC inspection before sealing:
      CQC1 = KQC1*CC*SZ
C           Electrical testing before sealing:
      CEPS = N*G*AVNTRU**0.1*CC
C           Troubleshooting before sealing:
      CTRUB = N*GPR*AVNTRU**0.1*CC
C           Reworking before sealing:
      CRWB = N*H*(G1*NC+G2*NWB)
C           2nd visual QC inspection before sealing:
      CQC2 = KQC2*CC*SZ
C           Sealing cost:
      CSL = L*SZ
C           Acceptance test after sealing:
      CACT = P*CT
C           Troubleshooting after sealing:
      CTRUA = NPR*GPR2*AVNTRU**0.1*CC
C           Reworking after sealing:
      CRWA = NPR*(HPR*(G1PR*NC+G2PR*NWB)+CLP)
C           Final quality control inspection:
      CQC3 = KQC3*SZ
C           Other steps:
      CO = 0.25
C     Assembly cost, volume-independent:
      CAP = (CPT+CBS+CBC+CWB+CND+CQC1+CEPS+CTRUB+CRWB
     2     +CQC2+CSL+CACT+CTRUA+CRWA+CQC3+CO)*NR
C     Assembly cost CFAT, volume-dependent:
      CFHAT = CA1*(P1+P2+1)*CC*GAMMA*V**BETA
C
C     IV.  R E C U R R I N G   M A T E R I A L   C O S T
      CP=23*TY*SZ*EXP(-7E-6*Q)! Package cost
      CCC=0.13*NTRU+0.80*NTRD ! Chip cost
     2   +1.6*NCAP
      CL=NPR*CLPR               ! Package lid cost
      CM=CP+CCC+CL
  100 COST(J,I)=CM+CERSP+CPRAT
C
      WRITE(IFLU,50)COST
      WRITE(IFLU,60)
      END
```

APPENDIX D

PRINTED WIRING BOARD (PWB) – COMPUTER PROGRAM TO CALCULATE SINGLE VALUED PWB COSTS

```
C       "PWB MANUFACTURING: Cost Modeling Program"
        REAL K,N1,N2,N3,NT
        DIMENSION IPPN(3),FORM(2)
        DOUBLE PRECISION FILNAM
        EQUIVALENCE (CASE,FORM(1))
        DATA FORM(2)/0/
        DATA IFLU/20/
C       This program computes the following values
C       and outputs them at the terminal and into
C       the data file 'special-case-name.DAT'
C       (FORTRAN Subroutine called: DCDFIL; execute
C       command EXECUTE PWBMAN.FOR,REL:SUP/LIB):
10      FORMAT (/,' PWB fabrication cost C''MFAB  = $ ',F6.2)
20      FORMAT (' PWB assembly cost C''MA  = $ ',F6.2,/)
30      FORMAT (' Recurring material fabrication cost: CMPF ',
     2           ' = $ ', F7.2)
40      FORMAT (' Recurring material assembly costs CMRA  ',
     2           ' = $ ', F7.2,/)
50      FORMAT(' Fabrication complexity factor CCFAB = ',F5.3)
60      FORMAT (' Assembly complexity factor CCA = ',F5.3,/)
70      FORMAT (' TOTAL MANUFACTURING COST CPWB = $ ', F8.2,/)
C
100     FORMAT (/,' PRINTED WIRING BOARD MANUFACTURE: ',/)
200     FORMAT (' Please select either of the following ',
     2     'as a special case : ',/,5X,' CARRI (Carrier) ', /,
     3     5X,' DIGIT (Digital) ',/,
     4     ' If neither type NONE: ', $)
210     FORMAT (A5)
220     FORMAT (5X,' Special case selected: ',A5)
230     FORMAT (5X,' Output file name: ',A10)
240     FORMAT (5X,' (CARRI = Carrier; DIGIT = Digital) ')
        TYPE 100
        TYPE 200
        ACCEPT 210,CASE
        TYPE 220,CASE
        CALL DCDFIL (CASE,'DAT',FILNAM,IPPN)
        TYPE 230,FILNAM
C
C       I.  G E N E R A L   C O S T   F A C T O R S
        K = 0.35            ! Slope
        PHI = 22.4          ! Facility size factor (intercept)
        PA1 = 0.2           ! Fraction of non-recurring assembly
C                             engineering costs
        PA2 = 0.35          ! Fraction of non-recurring materials
C                             assembly costs
        PF1 = 0.2           ! Fraction of non-recurring
C                             engineering costs
        PF2 = 0.25          ! Fraction of non-recurring
C                             materials costs
        V = 50              ! Yearly production volume
        SF = 0.5            ! Size factor, area
C
C       II. F A B R I C A T I O N
C       FABRICATION COST FACTORS:
        CLEAN = 0.5         ! Cleaning factor, PWB
        CMF = 1             ! Complexity of masking operation
        CPB = 0.015         ! Post-bake cost
        HD = 25             ! Hole density
        HDS = 3             ! Number of different hole sizes
        HN = 800            ! Number of holes
```

```
      HS = 32           ! Hole size
      LS = 10           ! Line spacing
      LW = 12           ! Line width
      NI = 10           ! Number of inspections
      IF (CASE.EQ.'CARRI')GO TO 250
      NL = 6            ! Number of layers
      GO TO 260
250   A = 0.37          ! CARRIER coefficient
      NL = 6*A
260   NRETC = 3         ! Number of retouchings, copper
      NRRPL = 1         ! Number of replatings
      NRPHR = 5         ! Number of photoresist retouchings
      NT = 50           ! Number of terminals
      PS = 40           ! Pad size
      PSF = 1           ! Press cycle factor
      PWBA = 30         ! PWB area, square inches
      QHF = 0.5         ! Hole quality factor
      QPLF = 0.5        ! Plating quality factor
      TAHF = 1          ! Adhesive type
      TCC = 1           ! Curing cycle
      TCUF = 1.75E-2    ! Copper thickness factor, SI.m/ounce
      THSF = 1          ! Type of heat sink
      TMAR = 1          ! Type of marking
      TMF = 1           ! Type of material
      TR = 0.05         ! Drilling tolerance
      TYR = 0.5         ! Type of photoresist
      WCU = 2           ! Weight of copper, ounces
      X = 0.23          ! Drilling tolerance (TR) exponent
      ALPHA = 1         ! CCFAB exponent
      BETA = 1          ! CCFAB exponent
      GAMMA = 1         ! CCFAB exponent
      DELTA = 1         ! CCFAB exponent
      CCFAB=(9.1E-3*HD+0.67*(1./LW+1./LS))**ALPHA! Fabrication
     2     +5*(1/PS)**BETA+1*(1/HS)**GAMMA        ! complexity
     3          +0.0125*NL**DELTA                 ! factor
C     FABRICATION STEPS:
      CCLE = 0.0133*NT                    ! Hot soak cleaning
      CPP = .16*TYR*SF*NL                 ! Photoprint
      CETC = CCFAB*0.86*NL*TCUF*WCU       ! Etching
      CPR = 5.5E-3*NL*CCFAB               ! Photoresist stripping
      CETA = 4.2E-3*NT                    ! Ethanol treatment
      CLAM = 2.5E-2*NL*TMF*PSF+CPP        ! Lamination and bake
      CDRL =.(3.4E-4*HN+0.19*HDS)*TR**X*QHF   ! Drilling
      CREM = 0.062*TMF*QHF*TCC            ! Removal of epoxy smear
      CELS=(6.25E-3*HS+0.008*HD)*CLEAN! Electroless plating
      CPL = 0.0111*CCFAB*HS               ! Electroplating
      CM = 0.006*TMAR                     ! Marking
      CHAR = 4.8E-3*NT*CCFAB              ! Installation of hardware
      CSRF = 0.226*QPLF                   ! Solder reflowing
      CPLC = 0.9*SF*CCFAB*CMF             ! Ni and Au plating
      CHS = 0.15*THSF*TAHF                ! Bond heat sink
      CINSPF = 8.8E-3*CCFAB*SF*NI         ! Inspection
      CETF = 1.2*CCFAB*SF                 ! Electrical testing
C     CRWF: Reworking after fabrication
      CRWF = 0.055*NRETC+0.166*NRRPI+0.0333*NRPHR
C
C     III.  A S S E M B L Y
C           ASSEMBLY COST FACTORS :
      AVCCC = 0.5       ! Average component complexity factor
      BF = 1            ! Bending factor
```

```
          CA1 = 0.056        ! Assembly complexity factor constant
          CA2 = 0.009        ! Assembly complexity factor constant
C         DAX = NAX/PWBA,    Axial component density
          DLAV = 26          ! Average lead density per component
C         DOT = NOTH/PWBA,   Other component density
          N = 1              ! Number of reworks
          N1 = 0.1           ! Fraction of hybrids reworked
          N2 = 0.02          ! Fraction of other components reworked
          N3 = 0.01          ! Fraction of solder joints
          NA = 2             ! Number of sides
          NAX = 80           ! Number of axial components
          NC = 94            ! Number of components
          NFP = 94           ! Number of flat packs
          NHY = 10           ! Number of hybrids
          NI = 5             ! Number of inspections
          NOTH = 14          ! Number of other components
          NSJ = 800          ! Number of solder joints
          NTR = 4            ! Number of transistors
          R = 1              ! Component type (1=axial; 0=other)
          RFORA = 60         ! Rate of forming of axial components/hr
          RFORFP = 1200      ! Rate of forming of flat packs per hour
          RFORH = 120        ! Rate of forming of hybrids per hour
          RFORT = 20         ! Rate of forming of transistors/hour
          RIA = 60           ! Rate of insertion of axial comps./hr
          RIFP = 1200        ! Rate of insertion of flat packs per hr
          RIH = 120          ! Rate of insertion of hybrids per hour
          RIT = 20           ! Rate of insertion of transistors/hour
          RLM = 500          ! Rate of loading per hour
          RLT = 50           ! Rate of leak test
          RTIN = 50          ! Rate of tinning per hour
          RVC = 100          ! Rate of vapor cleaning per hour
          Y = 1              ! Exponent of AVCCC
          DAX = NAX/PWBA
          DOT = NOTH/PWBA
          CCA = CA1*(DAX+DOT)+CA2*DLAV**1.1! Complexity factor
C                ASSEMBLY STEPS :
          CLF = NA*0.075*(NAX/RFORA+NTR/RFORT+NHY/RFORH)*BF
C              Lead forming
          IF(CASE.EQ.'DIGIT')CLF = (NFP/RFORFP)*BF
          CTIN = NA*0.06*NC/RTIN   ! Tinning
          CVC = NA*0.055*NC/RVC    ! Vapor cleaning
          CLT = NA*R*0.065*NC/RLT  ! Leak test
          CLM = NA*0.3*NC/RLM      ! Load magazines
          CCI = NA*0.15*(NAX/RIA+NTR/RIT+NHY/RIH)*BF
C              Component insertion on PWB panel
          IF(CASE.EQ.'DIGIT')CCI = (NFP/RIFP)*BF
          CRS = 0.03                ! Reflow soldering
          CETA = 0.88*AVCCC**Y*CCA! Electrical testing
          CTROB = 2.2*AVCCC**Y*CCA! Troubleshooting
C         CRWA: Reworking after assembly
          CRWA = N*(0.175*N1*NHY+0.054*N2*NOTH+0.011*N3*NSJ)
          CCT = 0.15*SF             ! Conformal coating
          CINSPA = NI*0.088*CCA*SF         ! Inspection
C
C         IV.  T O T A L   M A N U F A C T U R E
          WR = 20          ! wage rate, $/hour
C         CMRF, Recurring material fabrication costs:
          F = 1    ! Materials factor, fabrication
C                (1 = epoxy; 1.8 = polyimide)
          CMM = 2*F*NL*SF          !Material
```

```
        CMP = 0.36*F*NL*SF         !Prepreg
        CCH = 0.8                  !Chemicals
        CAU = 2.5                  !Gold bath
        CMPF = CMM + CMP + CCH + CAU
C       CMPA, Recurring material assembly costs:
C       Components cost factor:
        CCOMP=0.52*MAX+3.5*NTR+450*NHY ! Components
        B = 0.57           ! Components coefficient
        IF(CASE.EQ.'DIGIT')CCOMP=15*NFP
        IF(CASE.EQ.'CARRI')CCOMP=B*15*NFP
        CMO = 20           ! Material constant
        CMPA = CCOMP + CMO
C       CMFAB, Fabrication cost, volume-independent:
        CMFAB=(CCLE+CPH+CETC+CRR+CAPA+CLAM
     2        +CDPA+CPEM+CELS+CPL+CP +CHAR+CSHF
     3        +CPLC+CHS+CINSPF+CETF+CPWF)*RP
C       CPMFAB, Fabrication cost, volume-dependent:
        CPMFAB=CMFAB*(PF1+PF2+1)*CCFAB*PHI*V**(-K)
        IF(CASE.EQ.'CARRI')GO TO 300
C        Assembly costs:
C       CMA, volume-independent:
        CMA =(CTP+CTIM+CVC+CLT+CLM+CCI+CRS+CETA+CTHOB+
     2        CRWA+CCT+CINSPA)*RR
        GO TO 310
C               Special case "Carrier":
300     D=0.7
        CMA=((CLF+CTIM+CVC+CLT+CLM+CCI+CRS+CETA+CTHOB
     2     +CRWA+CCT+CINSPA)*(1+D)-(CLF+CTIM+CLT))*RR
C       CPMA, Volume-dependent:
310     CPRMA = CMA*(PA1+PA2+1)*PHI*V**(-K)*CCA
C       CPMB, TOTAL MANUFACTURING COST
        CPMB = CPMFAB+CPRMA+CMPF+CMPA
C
        TYPE 10, CPMFAB
        TYPE 20, CPRMA
        TYPE 30, CMPF
        TYPE 40, CMPA
        TYPE 50, CCFAB
        TYPE 60,CCA
        TYPE 70, CPMB
        OPEN (UNIT=IFLU,ACCESS='SEQOUT',MODE='ASCII',
     2        DEVICE='DSK',FILE=FILNAM)
        WRITE (IFLU,100)
        WRITE (IFLU,220)CASE
        WRITE (IFLU,240)
        WRITE (IFLU,10)CPMFAB
        WRITE (IFLU,20)CPRMA
        WRITE (IFLU,30)CMPF
        WRITE (IFLU,40)CMPA
        WRITE (IFLU,50)CCFAB
        WRITE (IFLU,60)CCA
        WRITE (IFLU,70)CPMB
        END
```

APPENDIX E

PRINTED WIRING BOARD (PWB) – COMPUTER PROGRAM TO CALCULATE PWB COST MATRICES FOR THE GENERATION OF COST SURFACES

```
C      "PWB MANUFACTURE: Matrix Program"
C      This program generates a matrix for use in plotting
C      PWB manufacturing costs as a function of two variables
C      (selected cost factors) on a 3D surface using the
C      Thermal process of the Analysis subsystem of CAD.
C      (FORTRAN subroutine called: DCDFIL; execute command:
C      EXECUTE PWBMAT.FOR,REL:SUB/LIB)
       IMPLICIT REAL(K,L,N)
       INTEGER IFLU,I,J
       DIMENSION IPPN(3), FNAME(5)
       DIMENSION CPWB(50,50)
       REAL*8 FILNAM
       DATA IFLU/20/
10     FORMAT (' PWB MANUFACTURE: Matrix Generation ')
20     FORMAT (' Enter output file name : ', $)
30     FORMAT (5A5)
40     FORMAT ('!TEST')
50     FORMAT (50G)
60     FORMAT ('*')
       TYPE 10
       TYPE 20
       ACCEPT 30,FNAME
       CALL DCDFIL (FNAME,'DAT',FILNAM,IPPN)
       OPEN (UNIT=IFLU, ACCESS='SEQOUT', MODE='ASCII',
     1      FILE=FILNAM, DIRECTORY=IPPN, DISPOSE='SAVE')
       WRITE(IFLU,40)
       DO 100 I=1,50
       DO 100 J=1,50
       NL = 0.5*I
       V = J*2
C
C      I. G E N E R A L   C O S T   F A C T O R S
       K = 0.35             ! Slope
       PHI = 22.4           ! Facility size factor (intercept)
       PA1 = 0.2            ! Fraction of non-recurring assembly
C                             engineering costs
       PA2 = 0.35           ! Fraction of non-recurring materials
C                             assembly costs
       PF1 = 0.2            ! Fraction of non-recurring
C                             engineering costs
       PF2 = 0.25           ! Fraction of non-recurring
C                             materials costs
C      V = matrix element, yearly production volume
       SF = 0.5             ! Size factor, area
C
C      II. F A B R I C A T I O N
C      FABRICATION COST FACTORS:
       CLEAN = 0.5          ! Cleaning factor, PWB
       CMF = 1              ! Complexity of masking operation
       CPB = 0.015          ! Post-bake cost
       HD = 25              ! Hole density
       HDS = 3              ! Number of different hole sizes
       HN = 800             ! Number of holes
       HS = 32              ! Hole size
       LS = 10              ! Line spacing
       LW = 12              ! Line width
       NI = 10              ! Number of inspections
C      NL = matrix element, Number of layers
       NRETC = 3            ! Number of retouchings, copper
       NRHPL = 1            ! Number of replatings
```

```
      NRPHR = 5          ! Number of photoresist retouchings
      NT = 50            ! Number of terminals
      PS = 40            ! Pad size
      PSF = 1            ! Press cycle factor
      PWBA = 30          ! PWB area, square inches
      QHF = 0.5          ! Hole quality factor
      QPLF = 0.5         ! Plating quality factor
      TAHF = 1           ! Adhesive type
      TCC = 1            ! Curing cycle
      TCUF = 1.75E-2     ! Copper thickness factor, STOH/ounce
      THSF = 1           ! Type of heat sink
      TMAR = 1           ! Type of marking
      TMF = 1            ! Type of material
      TR = 0.05          ! Drilling tolerance
      TYP = 0.5          ! Type of photoresist
      WCU = 2            ! Weight of copper, ounces
      X = 0.23           ! Drilling tolerance (TR) exponent
      ALPHA = 1          ! CCFAB exponent
      BETA = 1           ! CCFAB exponent
      GAMMA = 1          ! CCFAB exponent
      DELTA = 1          ! CCFAB exponent
      CCFAB=(2.1E-3*HD+0.67*(1./LS+1./LS))**ALPHA! Fabrication
     2      +5*(1/PS)**BETA+4*(1/HS)**GAMMA       ! complexity
     3        +0.0125*NL**DELTA                   ! factor
C     FABRICATION STEPS:
      CCIP = 0.0133*NT                    ! Hot soak cleaning
      CPH = .16*TYR*SF*NL                 ! Photoprint
      CETC = CCFAB*0.86*NL*TCUF*WCU       ! Etching
      CPR = 5.5E-3*NL*CCFAB               ! Photoresist stripping
      CETA = 4.2E-3*NT                    ! Ethanol treatment
      CLAM = 2.5E-2*NL*TMF*PSF+CPB        ! Lamination and bake
      CDRM = (5.4E-4*HN+0.09*HDS)*TR**X*QHF   ! Drilling
      CREM = 0.502*TMF*QHF*TCC            ! Removal of epoxy smear
      CELS=(6.25E-3*HS+0.008*HD)*CLEAN! Electroless plating
      CPL = 0.0111*CCFAB*HS               ! Electroplating
      CM = 0.016*TMAR                     ! Marking
      CHAR = 4.8E-3*NT*CCFAB              ! Installation of hardware
      CSRF = 0.226*QPLF                   ! Solder reflowing
      CPLC = 0.9*SF*CCFAB*CHF             ! Ni and Au plating
      CHS = 0.15*THSF*TAHF                ! Bond heat sink
      CINSPF = 8.8E-3*CCFAB*SF*NI         ! Inspection
      CETF = 1.2*CCFAB*SF                 ! Electrical testing
C     CRWF: Reworking after fabrication
      CRWF = 0.055*NFETC+0.165*NRHPT+0.0333*NRPHR
C
C     III.  A S S E M B L Y
C               ASSEMBLY COST FACTORS :
      AVCCC = 0.5        ! Average component complexity factor
      BF = 1             ! Bending factor
      CA1 = 0.056        ! Assembly complexity factor constant
      CA2 = 0.009        ! Assembly complexity factor constant
C     DAX = NAX/PWBA,    Axial component density
      DLAV = 26          ! Average lead density per component
C     DOT = NOTH/PWBA,   Other component density
      N = 1              ! Number of reworks
      N1 = 0.1           ! Fraction of hybrids reworked
      N2 = 0.02          ! Fraction of other components reworked
      N3 = 0.01          ! Fraction of solder joints
      NA = 2             ! Number of sides
      NAX = 80           ! Number of axial components
```

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      NC = 94           ! Number of components
      NFP = 94          ! Number of flat packs
      NHY = 10          ! Number of hybrids
      NI = 5            ! Number of inspections
      NOTH = 14         ! Number of other components
      NSJ = 800         ! Number of solder joints
      NTR = 4           ! Number of transistors
      R = 1             ! Component type (1=axial; 0=other)
      RFORA = 60        ! Rate of forming of axial components/hr
      RFORFP = 1200     ! Rate of forming of flat packs per hour
      RFORH = 120       ! Rate of forming of hybrids per hour
      RFORT = 20        ! Rate of forming of transistors/hour
      RIA = 60          ! Rate of insertion of axial comps./hr
      RIFP = 1200       ! Rate of insertion of flat packs per hr
      RIH = 120         ! Rate of insertion of hybrids per hour
      RIT = 20          ! Rate of insertion of transistors/hour
      RLM = 500         ! Rate of loading per hour
      RLT = 50          ! Rate of leak test
      RTIN = 50         ! Rate of tinning per hour
      RVC = 100         ! Rate of vapor cleaning per hour
      Y = 1             ! Exponent of AVCCC
      DAX = NAX/PWBA
      DOT = NOTH/PWBA
      CCA = CA1*(DAX+DOT)+CA2*DLAV**1.1! Complexity factor
C             ASSEMBLY STEPS :
      CLF = NA*0.075*(NAX/RFORA+NTR/RFORT+NHY/RFORH)*SF
C           Lead forming
      CTIN = NA*0.06*NC/RTIN  ! Tinning
      CVC = NA*0.055*NC/RVC   ! Vapor cleaning
      CLT = NA*R*0.065*NC/RLT ! Leak test
      CLM = NA*0.3*NC/RLM      ! Load magazines
      CCI = NA*0.15*(NAX/RIA+NTR/RIT+NHY/RIH)*SF
C     (CCI = Component insertion on PWB panel)
      CPS = 0.03               ! Reflow soldering
      CETA = 0.86*AVCCC**Y*CCA! Electrical testing
      CTROB = 2.2*AVCCC**Y*CCA! Troubleshooting
C     CRWA: Reworking after assembly
      CRWA = N*(0.175*N1*NHY+0.054*N2*NOTH+0.011*N3*NSJ)
      CCT = 0.15*SF            ! Conformal coating
      CINSPA = NI*0.088*CCA*SF        ! Inspection
C
C     IV.  T O T A L   M A N U F A C T U R E
      WR = 20          ! Wage rate, $/hour
C     CMRF, Recurring material fabrication costs:
      F = 1   ! Materials factor, fabrication
C              (1 = epoxy; 1.8 = polyimide)
      CMM = 2*F*NL*SF          !Material
      CMP = 0.36*F*NL*SF       !Prepreg
      CCH = 0.8                !Chemicals
      CAU = 2.5                !Gold bath
      CMRF = CMM + CMP + CCH + CAU
C     CMRA, Recurring material assembly costs:
C     Components cost factor:
      CCOMP=0.52*NAX+3.5*NTR+450*NHY ! Components
      COO = 20          ! Material constant
      CMRA = CCOMP + COO
C     CMFAB, Fabrication cost, volume-independent:
      CMFAB=(CCLE+CPH+CETC+CRR+CEPA+CLAM
     2.     +CDPM+CREM+CELS+CPL+CM+CHAR+CSRF
     3      +CPLC+CHS+CINSPF+CETF+CRWF)*WR
```

```
C       CPMFAB, Fabrication cost, volume-dependent:
        CPMFAB=CMFAB*(PF1+PF2+1)*CCFAB*PHI*V**(-K)
C        Assembly costs:
C       CMA, Volume-independent:
        CMA =(CIF+CTIM+CVC+CLT+CLM+CCI+CWS+CETA+CTROB+
        2        CRWA+CCT+CINSPA)*AR
C       CPMA, Volume-dependent:
        CPRMA = CMA*(PA1+PA2+1)*PHI*V**(-K)*CCA
C       CPMB, TOTAL MANUFACTURING COST
100     CPMB(J,I) = CPMFAB+CPRMA+CMPF+CMRA
        WRITE (IFLU,50)CPMB
        WRITE (IFLU,60)
        END
```